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EDA ESL startup Imperas close to launch

By Michael Santarini, Senior Editor -- 12/18/2007
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Over the last couple of years, there's been a lot of talk in the ESL niche of the EDA community about a small startup called Imperas Design. Since it's founding a couple of years ago, the company has been releasing only vague details about its product direction to the press but enough information to EDA analyst Gary Smith for him to describe it as having one of the most promising product directions in years. And that's pretty impressive, considering the company has yet to commercially release its first product. EDN has learned, however, that Imperas will introduce its product early next year, but has had to alter its focus a bit.

Certainly one of the reasons this startup has been raising expectations is because the company is being run by industry veteran Simon Davidmann, who has a track record for being with startups that have delivered significant innovations in design tools (and a knack for raising hype). Davidmann was a co-developer of the HILO language, the first RTL simulation language, which was acquired by GenRad, and was an early employee of Gateway Design Automation, the original developer of the Verilog hardware description language. Then after stints with several companies, Davidmann teamed up once again with some of the innovators from HILO and Gateway to found Co-Design, which developed Superlog, now known as SystemVerilog. Davidmann successfully sold that company to Synopsys a few years ago, and SystemVerilog has since become the de facto standard next generation HDL.

But instead of just retiring after selling Co-Design, Davidmann along with HILO and SystemVerilog co-developer Peter Flake immediately started working on a new company with high ambitions: a tool set to facilitate the programming and modeling of multi-processor core ICs.

Davidmann said the industry is littered with the bones of IC startups that created innovative multi-processor architectures but couldn't find a way to efficiently program the chips to work effectively. In other words, software development has become the bottleneck.

One of the biggest obstacles holding back multi-core processing has been modeling. There hasn't been a way to quickly develop processor models or a way to get models to run fast enough to allow architects and software designers to accurately create applications that take advantage of multi-processor architectures.

Thus, Imperas a few years ago set out to create a system that would do it. Initially, the company was planning on developing a tool suite to address all aspects of software

development for multi-core systems. Now, however, the company has paired back plans and will first introduce a simulation and debug system and add on development tools from there.

Davidmann said the company will first focus on offering a tool for multi-processing software virtual prototype that allows users to create an executable model of chip, do performance analysis and platform optimization. This includes multiprocessing simulation, user modeling and a model library.

Davidmann is quick to note that Imperas will not be a services company. "There are several virtual prototyping companies that tend to be services companies, where they will produce the model for you," he said. "But customers are saying 'that's just as bad as having a tapeout. We get the job done, then go away and after they've spent a lot of time talking to us, they give us model when we wanted it a year earlier.' The current solutions out there are either a service or they are too low level."

Davidmann said for example that SystemC is too low level and commercial tools are not appropriate for building processor models. "When you do get these environments to work, they are too slow," said Davidmann. "You want hundreds of million instructions per second to run an application. If you got a chip running three processors at 300 MHz, that's almost a thousand million instructions per second. A typical SystemC environment will run at 100 kilocycles to a million and that's 1000 times slower—you just can't develop software on that."

Davidmann declined to give specifics of its upcoming offerings but said the company isn't going to introduce a new language to speed up model development.

Along with the software virtual prototyping system, the company will also introduce application verification and debug environment targeted at multiprocessor core issues and quality. "Multicore processing presents all these new problems for the software guys," said Davidmann. "Yes, you have to partition it and parallelize it, but you have a lot of communication issues you have to address. You need to have programming but now software guys also need simulation. In the hardware world we simulate everything, but more and more software guys are going to have to start simulating their applications. That also means they are going to need software debug."

Davidmann said that originally company had planned to launch itself with two more tool offerings built on top of the MP Virtual Prototyping system and the verification and debug environment. Those offerings are a workbench, which is essentially an application programming environment to help companies manage, control, program and deliver multiprocessing application software and an ambitious tool that would provide users with a multiprocessing programming model composed of parallel application software that is correct by construction, automatically mapped and optimized to different hardware platforms.

“We think the market today is really in virtual prototyping systems, verification, and debug,” said Davidmann.

One of the big problems in the ESL space has traditionally been price points. That is, hardware design companies are used to shelling out lots of cash for tools, but software designers are used to getting tools for low or no cost. Davidmann said Imperas is and will sell its offerings to SOC companies and design groups that compose both hardware and software groups.

Davidmann said a few customers are already beta testing the tools, but the company is not planning on releasing more details of the software until it officially launches the tool sometime early next year.

Imperas was initially venture backed, but Davidmann said it recently went through a management buyout to control the company completely.

The company has 10 employees and has just brought on industry veteran EDA industry veteran Larry Lapides to head up sales.

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