OVP Guide to Using Processor Models

Model Specific Information for variant ARM_MultiCluster

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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1 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

This model implements an ARM system containing clusters of MPCore processors communicating using a common GICv2 or GICv3 block.
By default, the system contains Cortex-A53MPx4 and Cortex-A57MPx4 clusters, but this can be changed using parameter "override_clusterVariants". This parameter is a comma-separated list of cluster components (e.g. "Cortex-A53MPx4,Cortex-A57MPx4"). Note that if a GICv2 is selected, the total number of PEs must not exceed 8.

1.2 Licensing

This document describes the interface to the MultiCluster only. Refer to documentation of individual clusters for information regarding implemented features, licensing and limitations.

1.3 Limitations

1.4 Features

By default, the model implements a GICv2. Parameter enableGICv3 can be used to select a GICv3 instead.

2 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
arm.ovpworld.org/processor/arm/1.0

2.2 Asymmetric Multicore Processor

This processor contains more than one core of differing architectures

3 Other Variants in this Model

Table 1. All variants in this model

Variant
ARMv4T
ARMv4xM
ARMv4
ARMv4TxM
ARMv5xM
ARMv5
ARMv5TxM
ARMv5T

ARMv5TExP
ARMv5TE
ARMv5TEJ
ARMv6
ARMv6K
ARMv6T2
ARMv6KZ
ARMv7
ARM7TDMI
ARM7EJ-S
ARM720T
ARM920T
ARM922T
ARM926EJ-S
ARM940T
ARM946E
ARM966E
ARM968E-S
ARM1020E
ARM1022E
ARM1026EJ-S
ARM1136J-S
ARM1156T2-S
ARM1176JZ-S
Cortex-R4
Cortex-R4F
Cortex-A5UP
Cortex-A5MPx1
Cortex-A5MPx2
Cortex-A5MPx3
Cortex-A5MPx4
Cortex-A8
Cortex-A9UP
Cortex-A9MPx1
Cortex-A9MPx2
Cortex-A9MPx3
Cortex-A9MPx4
Cortex-A7UP
Cortex-A7MPx1
Cortex-A7MPx2
Cortex-A7MPx3
Cortex-A7MPx4

Cortex-A15UP
Cortex-A15MPx1
Cortex-A15MPx2
Cortex-A15MPx3
Cortex-A15MPx4
Cortex-A17MPx1
Cortex-A17MPx2
Cortex-A17MPx3
Cortex-A17MPx4
AArch32
AArch64
Cortex-A32MPx1
Cortex-A32MPx2
Cortex-A32MPx3
Cortex-A32MPx4
Cortex-A35MPx1
Cortex-A35MPx2
Cortex-A35MPx3
Cortex-A35MPx4
Cortex-A53MPx1
Cortex-A53MPx2
Cortex-A53MPx3
Cortex-A53MPx4
Cortex-A55MPx1
Cortex-A55MPx2
Cortex-A55MPx3
Cortex-A55MPx4
Cortex-A57MPx1
Cortex-A57MPx2
Cortex-A57MPx3
Cortex-A57MPx4
Cortex-A72MPx1
Cortex-A72MPx2
Cortex-A72MPx3
Cortex-A72MPx4
Cortex-A73MPx1
Cortex-A73MPx2
Cortex-A73MPx3
Cortex-A73MPx4
Cortex-A75MPx1
Cortex-A75MPx2
Cortex-A75MPx3

Cortex-A75MPx4
MultiCluster

4 Bus Ports

Table 2. Bus Ports

Type	Name	min	max	Description
master (initiator)	INSTRUCTION	32	53	
master (initiator)	DATA	32	53	
master (initiator)	GICRegisters	32	32	GIC memory-mapped register block

5 Net Ports

Table 3. Net Ports

Name	Type	Description
SPI32	input	Shared peripheral interrupt
SPI33	input	Shared peripheral interrupt
SPI34	input	Shared peripheral interrupt
SPI35	input	Shared peripheral interrupt
SPI36	input	Shared peripheral interrupt
SPI37	input	Shared peripheral interrupt
SPI38	input	Shared peripheral interrupt
SPI39	input	Shared peripheral interrupt
SPI40	input	Shared peripheral interrupt
SPI41	input	Shared peripheral interrupt
SPI42	input	Shared peripheral interrupt
SPI43	input	Shared peripheral interrupt
SPI44	input	Shared peripheral interrupt
SPI45	input	Shared peripheral interrupt
SPI46	input	Shared peripheral interrupt
SPI47	input	Shared peripheral interrupt
SPI48	input	Shared peripheral interrupt
SPI49	input	Shared peripheral interrupt
SPI50	input	Shared peripheral interrupt
SPI51	input	Shared peripheral interrupt
SPI52	input	Shared peripheral interrupt
SPI53	input	Shared peripheral interrupt
SPI54	input	Shared peripheral interrupt
SPI55	input	Shared peripheral interrupt
SPI56	input	Shared peripheral interrupt
SPI57	input	Shared peripheral interrupt
SPI58	input	Shared peripheral interrupt
SPI59	input	Shared peripheral interrupt

SPI60	input	Shared peripheral interrupt
SPI61	input	Shared peripheral interrupt
SPI62	input	Shared peripheral interrupt
SPI63	input	Shared peripheral interrupt
SPI64	input	Shared peripheral interrupt
SPI65	input	Shared peripheral interrupt
SPI66	input	Shared peripheral interrupt
SPI67	input	Shared peripheral interrupt
SPI68	input	Shared peripheral interrupt
SPI69	input	Shared peripheral interrupt
SPI70	input	Shared peripheral interrupt
SPI71	input	Shared peripheral interrupt
SPI72	input	Shared peripheral interrupt
SPI73	input	Shared peripheral interrupt
SPI74	input	Shared peripheral interrupt
SPI75	input	Shared peripheral interrupt
SPI76	input	Shared peripheral interrupt
SPI77	input	Shared peripheral interrupt
SPI78	input	Shared peripheral interrupt
SPI79	input	Shared peripheral interrupt
SPI80	input	Shared peripheral interrupt
SPI81	input	Shared peripheral interrupt
SPI82	input	Shared peripheral interrupt
SPI83	input	Shared peripheral interrupt
SPI84	input	Shared peripheral interrupt
SPI85	input	Shared peripheral interrupt
SPI86	input	Shared peripheral interrupt
SPI87	input	Shared peripheral interrupt
SPI88	input	Shared peripheral interrupt
SPI89	input	Shared peripheral interrupt
SPI90	input	Shared peripheral interrupt
SPI91	input	Shared peripheral interrupt
SPI92	input	Shared peripheral interrupt
SPI93	input	Shared peripheral interrupt
SPI94	input	Shared peripheral interrupt
SPI95	input	Shared peripheral interrupt
SPIVector	input	Shared peripheral interrupt vectorized input
periphReset	input	Peripheral reset (active high)
CFGSDISABLE	input	Secure configuration lockdown (active high)
GICCDISABLE	input	GIC CPU interface logic disable (active high, sampled on rising edge of periphReset)
EVENTI	input	Event input signal, active on rising edge

EVENTO	output	Event output signal, active on rising edge
PPI16_C0_0	input	Private peripheral interrupt
PPI17_C0_0	input	Private peripheral interrupt
PPI18_C0_0	input	Private peripheral interrupt
PPI19_C0_0	input	Private peripheral interrupt
PPI20_C0_0	input	Private peripheral interrupt
PPI21_C0_0	input	Private peripheral interrupt
PPI22_C0_0	input	Private peripheral interrupt
PPI23_C0_0	input	Private peripheral interrupt
PPI24_C0_0	input	Private peripheral interrupt
PPI25_C0_0	input	Private peripheral interrupt
PPI26_C0_0	input	Private peripheral interrupt
PPI27_C0_0	input	Private peripheral interrupt
PPI28_C0_0	input	Private peripheral interrupt
PPI29_C0_0	input	Private peripheral interrupt
PPI30_C0_0	input	Private peripheral interrupt
PPI31_C0_0	input	Private peripheral interrupt
CNTVIRQ_C0_0	output	Virtual timer event (active high)
CNTPSIRQ_C0_0	output	Secure physical timer event (active high)
CNTPNSIRQ_C0_0	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_0	output	Hypervisor physical timer event (active high)
IRQOUT_C0_0	output	IRQ wakeup
FIQOUT_C0_0	output	FIQ wakeup
CLUSTERIDAFF1_C0	input	Configure MPIDR.Aff1
CLUSTERIDAFF2_C0	input	Configure MPIDR.Aff2
VINITHI_C0_0	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_0	input	Configure exception endianness (SCTLR.EE)
CFGTE_C0_0	input	Configure exception state at reset (SCTLR.TE)
reset_C0_0	input	Processor reset, active high
fiq_C0_0	input	FIQ interrupt, active high (negation of nFIQ)
irq_C0_0	input	IRQ interrupt, active high (negation of nIRQ)
sei_C0_0	input	System error interrupt, active high
vfiq_C0_0	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_0	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_0	input	Virtual system error interrupt, active high
AXI_SLVERR_C0_0	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_0	input	CP15SDISABLE (active high)
PMUIRQ_C0_0	output	Performance monitor event (active high)
SMPEN_C0_0	output	CPUECTLR.SMPEN current value
PPI16_C0_1	input	Private peripheral interrupt

PPI17_C0_1	input	Private peripheral interrupt
PPI18_C0_1	input	Private peripheral interrupt
PPI19_C0_1	input	Private peripheral interrupt
PPI20_C0_1	input	Private peripheral interrupt
PPI21_C0_1	input	Private peripheral interrupt
PPI22_C0_1	input	Private peripheral interrupt
PPI23_C0_1	input	Private peripheral interrupt
PPI24_C0_1	input	Private peripheral interrupt
PPI25_C0_1	input	Private peripheral interrupt
PPI26_C0_1	input	Private peripheral interrupt
PPI27_C0_1	input	Private peripheral interrupt
PPI28_C0_1	input	Private peripheral interrupt
PPI29_C0_1	input	Private peripheral interrupt
PPI30_C0_1	input	Private peripheral interrupt
PPI31_C0_1	input	Private peripheral interrupt
CNTVIRQ_C0_1	output	Virtual timer event (active high)
CNTPSIRQ_C0_1	output	Secure physical timer event (active high)
CNTPNSIRQ_C0_1	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_1	output	Hypervisor physical timer event (active high)
IRQOUT_C0_1	output	IRQ wakeup
FIQOUT_C0_1	output	FIQ wakeup
VINITHI_C0_1	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_1	input	Configure exception endianness (SCTLR.EE)
CFGTE_C0_1	input	Configure exception state at reset (SCTLR.TE)
reset_C0_1	input	Processor reset, active high
fiq_C0_1	input	FIQ interrupt, active high (negation of nFIQ)
irq_C0_1	input	IRQ interrupt, active high (negation of nIRQ)
sei_C0_1	input	System error interrupt, active high
vfiq_C0_1	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_1	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_1	input	Virtual system error interrupt, active high
AXI_SLVERR_C0_1	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_1	input	CP15SDISABLE (active high)
PMUIRQ_C0_1	output	Performance monitor event (active high)
SMPEN_C0_1	output	CPUECTLR.SMPEN current value
PPI16_C0_2	input	Private peripheral interrupt
PPI17_C0_2	input	Private peripheral interrupt
PPI18_C0_2	input	Private peripheral interrupt
PPI19_C0_2	input	Private peripheral interrupt
PPI20_C0_2	input	Private peripheral interrupt

PPI21_C0_2	input	Private peripheral interrupt
PPI22_C0_2	input	Private peripheral interrupt
PPI23_C0_2	input	Private peripheral interrupt
PPI24_C0_2	input	Private peripheral interrupt
PPI25_C0_2	input	Private peripheral interrupt
PPI26_C0_2	input	Private peripheral interrupt
PPI27_C0_2	input	Private peripheral interrupt
PPI28_C0_2	input	Private peripheral interrupt
PPI29_C0_2	input	Private peripheral interrupt
PPI30_C0_2	input	Private peripheral interrupt
PPI31_C0_2	input	Private peripheral interrupt
CNTVIRQ_C0_2	output	Virtual timer event (active high)
CNTPSIRQ_C0_2	output	Secure physical timer event (active high)
CNTPNSIRQ_C0_2	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_2	output	Hypervisor physical timer event (active high)
IRQOUT_C0_2	output	IRQ wakeup
FIQOUT_C0_2	output	FIQ wakeup
VINITHI_C0_2	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_2	input	Configure exception endianness (SCTLR.EE)
CFGTE_C0_2	input	Configure exception state at reset (SCTLR.TE)
reset_C0_2	input	Processor reset, active high
fiq_C0_2	input	FIQ interrupt, active high (negation of nFIQ)
irq_C0_2	input	IRQ interrupt, active high (negation of nIRQ)
sei_C0_2	input	System error interrupt, active high
vfiq_C0_2	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_2	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_2	input	Virtual system error interrupt, active high
AXI_SLVERR_C0_2	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_2	input	CP15SDISABLE (active high)
PMUIRQ_C0_2	output	Performance monitor event (active high)
SMPEN_C0_2	output	CPUECTLR.SMPEN current value
PPI16_C0_3	input	Private peripheral interrupt
PPI17_C0_3	input	Private peripheral interrupt
PPI18_C0_3	input	Private peripheral interrupt
PPI19_C0_3	input	Private peripheral interrupt
PPI20_C0_3	input	Private peripheral interrupt
PPI21_C0_3	input	Private peripheral interrupt
PPI22_C0_3	input	Private peripheral interrupt
PPI23_C0_3	input	Private peripheral interrupt
PPI24_C0_3	input	Private peripheral interrupt

PPI25_C0_3	input	Private peripheral interrupt
PPI26_C0_3	input	Private peripheral interrupt
PPI27_C0_3	input	Private peripheral interrupt
PPI28_C0_3	input	Private peripheral interrupt
PPI29_C0_3	input	Private peripheral interrupt
PPI30_C0_3	input	Private peripheral interrupt
PPI31_C0_3	input	Private peripheral interrupt
CNTVIRQ_C0_3	output	Virtual timer event (active high)
CNTPSIRQ_C0_3	output	Secure physical timer event (active high)
CNTPNSIRQ_C0_3	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C0_3	output	Hypervisor physical timer event (active high)
IRQOUT_C0_3	output	IRQ wakeup
FIQOUT_C0_3	output	FIQ wakeup
VINITHI_C0_3	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C0_3	input	Configure exception endianness (SCTLR.EE)
CFGTE_C0_3	input	Configure exception state at reset (SCTLR.TE)
reset_C0_3	input	Processor reset, active high
fiq_C0_3	input	FIQ interrupt, active high (negation of nFIQ)
irq_C0_3	input	IRQ interrupt, active high (negation of nIRQ)
sei_C0_3	input	System error interrupt, active high
vfiq_C0_3	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C0_3	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C0_3	input	Virtual system error interrupt, active high
AXI_SLVERR_C0_3	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C0_3	input	CP15SDISABLE (active high)
PMUIRQ_C0_3	output	Performance monitor event (active high)
SMPEN_C0_3	output	CPUECTLR.SMPEN current value
PPI16_C1_0	input	Private peripheral interrupt
PPI17_C1_0	input	Private peripheral interrupt
PPI18_C1_0	input	Private peripheral interrupt
PPI19_C1_0	input	Private peripheral interrupt
PPI20_C1_0	input	Private peripheral interrupt
PPI21_C1_0	input	Private peripheral interrupt
PPI22_C1_0	input	Private peripheral interrupt
PPI23_C1_0	input	Private peripheral interrupt
PPI24_C1_0	input	Private peripheral interrupt
PPI25_C1_0	input	Private peripheral interrupt
PPI26_C1_0	input	Private peripheral interrupt
PPI27_C1_0	input	Private peripheral interrupt
PPI28_C1_0	input	Private peripheral interrupt

PPI29_C1_0	input	Private peripheral interrupt
PPI30_C1_0	input	Private peripheral interrupt
PPI31_C1_0	input	Private peripheral interrupt
CNTVIRQ_C1_0	output	Virtual timer event (active high)
CNTPSIRQ_C1_0	output	Secure physical timer event (active high)
CNTPNSIRQ_C1_0	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_0	output	Hypervisor physical timer event (active high)
IRQOUT_C1_0	output	IRQ wakeup
FIQOUT_C1_0	output	FIQ wakeup
CLUSTERIDAFF1_C1	input	Configure MPIDR.Aff1
CLUSTERIDAFF2_C1	input	Configure MPIDR.Aff2
VINITHI_C1_0	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_0	input	Configure exception endianness (SCTLR.EE)
CFGTE_C1_0	input	Configure exception state at reset (SCTLR.TE)
reset_C1_0	input	Processor reset, active high
fiq_C1_0	input	FIQ interrupt, active high (negation of nFIQ)
irq_C1_0	input	IRQ interrupt, active high (negation of nIRQ)
sei_C1_0	input	System error interrupt, active high
vfiq_C1_0	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_0	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_0	input	Virtual system error interrupt, active high
AXI_SLVERR_C1_0	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_0	input	CP15SDISABLE (active high)
PMUIRQ_C1_0	output	Performance monitor event (active high)
SMPEN_C1_0	output	CPUECTLR.SMPEN current value
PPI16_C1_1	input	Private peripheral interrupt
PPI17_C1_1	input	Private peripheral interrupt
PPI18_C1_1	input	Private peripheral interrupt
PPI19_C1_1	input	Private peripheral interrupt
PPI20_C1_1	input	Private peripheral interrupt
PPI21_C1_1	input	Private peripheral interrupt
PPI22_C1_1	input	Private peripheral interrupt
PPI23_C1_1	input	Private peripheral interrupt
PPI24_C1_1	input	Private peripheral interrupt
PPI25_C1_1	input	Private peripheral interrupt
PPI26_C1_1	input	Private peripheral interrupt
PPI27_C1_1	input	Private peripheral interrupt
PPI28_C1_1	input	Private peripheral interrupt
PPI29_C1_1	input	Private peripheral interrupt
PPI30_C1_1	input	Private peripheral interrupt

PPI31_C1_1	input	Private peripheral interrupt
CNTVIRQ_C1_1	output	Virtual timer event (active high)
CNTPSIRQ_C1_1	output	Secure physical timer event (active high)
CNTPNSIRQ_C1_1	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_1	output	Hypervisor physical timer event (active high)
IRQOUT_C1_1	output	IRQ wakeup
FIQOUT_C1_1	output	FIQ wakeup
VINITHI_C1_1	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_1	input	Configure exception endianness (SCTLR.EE)
CFGTE_C1_1	input	Configure exception state at reset (SCTLR.TE)
reset_C1_1	input	Processor reset, active high
fiq_C1_1	input	FIQ interrupt, active high (negation of nFIQ)
irq_C1_1	input	IRQ interrupt, active high (negation of nIRQ)
sei_C1_1	input	System error interrupt, active high
vfiq_C1_1	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_1	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_1	input	Virtual system error interrupt, active high
AXI_SLVERR_C1_1	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_1	input	CP15SDISABLE (active high)
PMUIRQ_C1_1	output	Performance monitor event (active high)
SMPEN_C1_1	output	CPUECTLR.SMPEN current value
PPI16_C1_2	input	Private peripheral interrupt
PPI17_C1_2	input	Private peripheral interrupt
PPI18_C1_2	input	Private peripheral interrupt
PPI19_C1_2	input	Private peripheral interrupt
PPI20_C1_2	input	Private peripheral interrupt
PPI21_C1_2	input	Private peripheral interrupt
PPI22_C1_2	input	Private peripheral interrupt
PPI23_C1_2	input	Private peripheral interrupt
PPI24_C1_2	input	Private peripheral interrupt
PPI25_C1_2	input	Private peripheral interrupt
PPI26_C1_2	input	Private peripheral interrupt
PPI27_C1_2	input	Private peripheral interrupt
PPI28_C1_2	input	Private peripheral interrupt
PPI29_C1_2	input	Private peripheral interrupt
PPI30_C1_2	input	Private peripheral interrupt
PPI31_C1_2	input	Private peripheral interrupt
CNTVIRQ_C1_2	output	Virtual timer event (active high)
CNTPSIRQ_C1_2	output	Secure physical timer event (active high)
CNTPNSIRQ_C1_2	output	Non-secure physical timer event (active high)

CNTPHPIRQ_C1_2	output	Hypervisor physical timer event (active high)
IRQOUT_C1_2	output	IRQ wakeup
FIQOUT_C1_2	output	FIQ wakeup
VINITHI_C1_2	input	Configure HIVECS mode (SCTLR.V)
CFGEND_C1_2	input	Configure exception endianness (SCTLR.EE)
CFGTE_C1_2	input	Configure exception state at reset (SCTLR.TE)
reset_C1_2	input	Processor reset, active high
fiq_C1_2	input	FIQ interrupt, active high (negation of nFIQ)
irq_C1_2	input	IRQ interrupt, active high (negation of nIRQ)
sei_C1_2	input	System error interrupt, active high
vfiq_C1_2	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_2	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_2	input	Virtual system error interrupt, active high
AXI_SLVERR_C1_2	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_2	input	CP15SDISABLE (active high)
PMUIRQ_C1_2	output	Performance monitor event (active high)
SMPEN_C1_2	output	CPUECTLR.SMPEN current value
PPI16_C1_3	input	Private peripheral interrupt
PPI17_C1_3	input	Private peripheral interrupt
PPI18_C1_3	input	Private peripheral interrupt
PPI19_C1_3	input	Private peripheral interrupt
PPI20_C1_3	input	Private peripheral interrupt
PPI21_C1_3	input	Private peripheral interrupt
PPI22_C1_3	input	Private peripheral interrupt
PPI23_C1_3	input	Private peripheral interrupt
PPI24_C1_3	input	Private peripheral interrupt
PPI25_C1_3	input	Private peripheral interrupt
PPI26_C1_3	input	Private peripheral interrupt
PPI27_C1_3	input	Private peripheral interrupt
PPI28_C1_3	input	Private peripheral interrupt
PPI29_C1_3	input	Private peripheral interrupt
PPI30_C1_3	input	Private peripheral interrupt
PPI31_C1_3	input	Private peripheral interrupt
CNTVIRQ_C1_3	output	Virtual timer event (active high)
CNTPSIRQ_C1_3	output	Secure physical timer event (active high)
CNTPNSIRQ_C1_3	output	Non-secure physical timer event (active high)
CNTPHPIRQ_C1_3	output	Hypervisor physical timer event (active high)
IRQOUT_C1_3	output	IRQ wakeup
FIQOUT_C1_3	output	FIQ wakeup
VINITHI_C1_3	input	Configure HIVECS mode (SCTLR.V)

CFGEND_C1_3	input	Configure exception endianness (SCTLR.EE)
CFGTE_C1_3	input	Configure exception state at reset (SCTLR.TE)
reset_C1_3	input	Processor reset, active high
fiq_C1_3	input	FIQ interrupt, active high (negation of nFIQ)
irq_C1_3	input	IRQ interrupt, active high (negation of nIRQ)
sei_C1_3	input	System error interrupt, active high
vfiq_C1_3	input	Virtual FIQ interrupt, active high (negation of nVFIQ)
virq_C1_3	input	Virtual IRQ interrupt, active high (negation of nVIRQ)
vsei_C1_3	input	Virtual system error interrupt, active high
AXI_SLVERR_C1_3	input	AXI external abort type (DECERR=0, SLVERR=1)
CP15SDISABLE_C1_3	input	CP15SDISABLE (active high)
PMUIRQ_C1_3	output	Performance monitor event (active high)
SMPEN_C1_3	output	CPUECTLR.SMPEN current value

6 FIFO Ports

No FIFO Ports in this model.

7 Parameters

Table 4. Parameters that can be set in the model, type: CLUSTER_GROUP

Name	Type	Description
disableGICModel	Boolean	Disable the internal GIC model entirely
enableGICv3	Boolean	Enable/disable GICv3 support
supportSTATUSR	Boolean	Enable/disable support for GICv3 GIC[CDV]_STATUSR registers
distinctMTCores	Boolean	For multi-threaded (MT) processors, simulate threads as separate cores (otherwise, simulate MT threads as a single entity)
override_clusterVariants	String	Specifies a comma-separated list of cluster variant names in this multicluster
override_timerScaleFactor	Uns32	Specifies the fraction of MIPS rate to use for MPCore timers (generic timers or global/local/ watchdogs depending on implementation). Defaults to 20 for generic timers, 2 for others
override_GICD_NSACRPresent	Boolean	Specifies that optional GICD_NSACR distributor registers are present (GICv2 only)
override_GICD_PPISRPresent	Boolean	Specifies that implementation-specific GICD_PPISR distributor register is present (GICv1 ICDPPIS/ICPPISR, GICv1 and GICv2 only)
override_GICD_SPISRPresent	Boolean	Specifies that implementation-specific GICD_SPISR distributor registers are present (GICv1 ICDSPIS/ICSPISR)

override_GICv3_DistributorBase	Uns64	Specify distributor register block base address (GICv3 only)
override_GICv3_E1NWFPresent	Boolean	Specifies that GICR_CTLR.E1NWF is implemented (GICv3 only)
override_GIC_PPIMask	Uns32	Specify bitmask of implemented PPIs in the GIC (e.g. ID16 is 0x0001, ID31 is 0x8000)
override_GICCDISABLE	Boolean	Specify initial value of GICCDISABLE
override_GICC_IIDR	Uns32	Override GICC_IIDR register (GICv1 ICCIIDR)
override_GICD_TYPER	Uns32	Override GICD_TYPER register (GICv1 ICDICTR)
override_GICD_TYPER_ITLines	Uns32	Override ITLinesNumber field of GICD_TYPER register (GICv1 ICDICTR)
override_GICD_ICFGRN	Uns32	Override reset value of GICD_ICFGR2...GICD_ICFGRn (GICv1 ICDICFR2...ICDICFRn)
override_GICD_IIDR	Uns32	Override GICD_IIDR register (GICv1 ICDIIDR)
override_GICH_VTR	Uns32	Override GICH_VTR register
override_GICR_IIDR	Uns32	Override GICR_IIDR register (GICv3 and later)
override_GITS_IIDR	Uns32	Override GITS_IIDR register (GICv3 and later)
override_GITS_TYPER	Uns64	Override GITS_TYPER register (GICv3 and later)
override_ICCPMRBits	Uns32	Specify the number of writable bits in GICC_PMR (GICv1 ICCPMR)
override_minICCBPR	Uns32	Specify the minimum possible value for GICC_BPR (GICv1 ICCBPR)

8 Model Commands

8.1 Level 1: CLUSTER_GROUP

8.1.1 isync

specify instruction address range for synchronous execution

Table 5. isync command arguments

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

8.1.2 itrace

enable or disable instruction tracing

Table 6. itrace command arguments

Argument	Type	Description
-after	Uns64	apply after this many instructions

-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

9 Registers

9.1 Level 1: CLUSTER_GROUP

No registers.
#

