OVP Guide to Using Processor Models

Model specific information for ARM_Cortex-M0plus

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Contents

Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

ARMM Processor Model

1.2 Licensing

Usage of binary model under license governing simulator usage.

Note that for models of ARM CPUs the license includes the following terms:

Licensee is granted a non-exclusive, worldwide, non-transferable, revocable licence to:

If no source is being provided to the Licensee: use and copy only (no modifications rights are granted) the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used

to emulate an ARM based system to run application software in a production or live environment.

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In the case of any Licensee who is either or both an academic or educational institution the purposes shall be limited to internal use.

Except to the extent that such activity is permitted by applicable law, Licensee shall not reverse engineer, decompile, or disassemble this model. If this model was provided to Licensee in Europe, Licensee shall not reverse engineer, decompile or disassemble the Model for the purposes of error correction.

The License agreement does not entitle Licensee to manufacture in silicon any product based on this model.

The License agreement does not entitle Licensee to use this model for evaluating the validity of any ARM patent.

The License agreement does not entitle Licensee to use the model to emulate an ARM based system to run application software in a production or live environment.

Source of model available under separate Imperas Software License Agreement.

1.3 Limitations

Performance Monitors are not implemented.

Debug Extension and related blocks are not implemented.

1.4 Verification

Models have been extensively tested by Imperas. ARM Cortex-M models have been successfully used by customers to simulate the Micrium uC/OS-II kernel and FreeRTOS.

1.5 Features

The model is configured with 16 interrupts and 2 priority bits (use override_numInterrupts parameter to change the number of interrupts; the number of priority bits is fixed in this profile).

Thumb instructions are supported.

MPU is present. Use parameter override_MPU_TYPE to disable it or change the number of MPU regions if required.

SysTick timer is present. Use parameter SysTickPresent to disable it if required.

Unprivileged/Privileged Extension is present. Use parameter unprivilegedExtension to disable it if required.

VTOR register is present. Use parameter VTORPresent to disable it if required.

Chapter 2

Configuration

2.1 Location

This model's VLNV is arm.ovpworld.org/processor/armm/1.0.
The model source is usually at:
$IMPERAS_HOME/ImperasLib/source/arm.ovpworld.org/processor/armm/1.0
The model binary is usually at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/arm.ovpworld.org/processor/armm/1.0

2.2 GDB Path

The default GDB for this model is: $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/arm-none-eabi-gdb.

2.3 Semi-Host Library

The default semi-host library file is arm.ovpworld.org/semihosting/armNewlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: 0x28.

Chapter 3

All Variants in this model

This model has these variants

Variant	Description
ARMv6-M	
ARMv7-M	
Cortex-M0	
Cortex-M0plus	(described in this document)
Cortex-M1	
Cortex-M3	
Cortex-M4	
Cortex-M4F	

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	32	32	mandatory	
DATA	32	32	optional	

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
sysResetReq	output	optional	
intISS	output	optional	
eventOut	output	optional	
lockup	output	optional	
int	input	optional	
reset	input	optional	
nmi	input	optional	
eventIn	input	optional	
int0	input	optional	
int1	input	optional	
int2	input	optional	
int3	input	optional	
int4	input	optional	
int5	input	optional	
int6	input	optional	
int7	input	optional	
int8	input	optional	
int9	input	optional	
int10	input	optional	
int11	input	optional	
int12	input	optional	
int13	input	optional	
int14	input	optional	
int15	input	optional	

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

Name	Type	Description
variant	Enumeration	Selects variant (either a generic ISA or a specific model)
verbose	Boolean	Specify verbosity of output
showHiddenRegs	Boolean	Show hidden registers during register tracing
UAL	Boolean	Disassemble using UAL syntax
compatibility	Enumeration	Specify compatibility mode(ISA, gdb or nopBKPT)
override_debugMask	Uns32	Specifies debug mask, enabling debug output for model components
endian	Endian	Model endian
instructionEndian	Endian	The architecture specifies that instruction fetch is always little endian; this attribute allows the defined instruction endianness to be overridden if required
resetAtTime0	Boolean	Reset the model at time=0 (default=1)
unprivilegedExtension	Boolean	Specify presence of Unprivileged/Privileged Extension
VTORPresent	Boolean	Specify presence of VTOR register
SysTickPresent	Boolean	Specify presence of SysTick timer
override_CPUID	Uns32	Override system CPUID register
override_MPU_TYPE	Uns32	Override system MPU_TYPE register
override_VTOR	Uns32	Override VTOR register reset value
override_STRoffsetPC12	Uns32	Specifies that STR/STR of PC should do so with 12:byte offset from the current instruction (if 1), otherwise an 8:byte offset is used
override_ERG	Uns32	Specifies exclusive reservation granule
override_numInterrupts	Uns32	Specifies number of external interrupt lines

Table 8.1: Parameters

Chapter 9

Execution Modes

Mode	Code
Thread	0
Handler	1

Table 9.1: Modes implemented in this processor

Chapter 10

Exceptions

Exception	Code
None	0
Reset	1
NMI	2
HardFault	3
SVCall	11
PendSV	14
SysTick	15
ExternalInt000	16
ExternalInt001	17
ExternalInt002	18
ExternalInt003	19
ExternalInt004	20
ExternalInt005	21
ExternalInt006	22
ExternalInt007	23
ExternalInt008	24
ExternalInt009	25
ExternalInt00a	26
ExternalInt00b	27
ExternalInt00c	28
ExternalInt00d	29
ExternalInt00e	30
ExternalInt00f	31

Table 10.1: Exceptions implemented by this processor

Chapter 11

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.
This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1

This level in the model hierarchy has 3 commands.
This level in the model hierarchy has 4 register groups:

Group name	Registers
Core	16
Control	5
System	31
Integration_support	2

Table 11.1: Register groups

This level in the model hierarchy has no children.

Chapter 12

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1

12.1.1 debugflags

show or modify the processor debug flags

Argument	Type	Description
-get	Boolean	print current processor flags value
-mask	Boolean	print current processor flags value
-set	Int32	new processor flags (only flags 0x0000008c can be modified)

Table 12.1: debugflags command arguments

12.1.2 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.2: isync command arguments

12.1.3 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing

-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.3: itrace command arguments

Chapter 13

Registers

13.1 Level 1

13.1.1 Core

Registers at level:1, group:Core

Name	Bits	Initial-Hex	RW	Description
r0	32	0	rw	
r1	32	0	rw	
r2	32	0	rw	
r3	32	0	rw	
r4	32	0	rw	
r5	32	0	rw	
r6	32	0	rw	
r7	32	0	rw	
r8	32	0	rw	
r9	32	0	rw	
r10	32	0	rw	
r11	32	0	rw	frame pointer
r12	32	0	rw	
sp	32	0	rw	stack pointer
lr	32	0	rw	
pc	32	0	rw	program counter

Table 13.1: Registers at level 1, group:Core

13.1.2 Control

Registers at level:1, group:Control

Name	Bits	Initial-Hex	RW	Description
cpsr	32	0	rw	xPSR register. Includes APSR, IPSR and EPSR
control	32	0	rw	
primask	32	0	rw	
sp_process	32	0	rw	stack pointer
sp_main	32	0	rw	stack pointer

Table 13.2: Registers at level 1, group:Control

13.1.3 System

Registers at level:1, group:System

Name	Bits	Initial-Hex	RW	Description
ACTLR	32	0	rw	Address 0xe000e008
SYST_CSR	32	4	rw	Address 0xe000e010
SYST_RVR	32	0	rw	Address 0xe000e014
SYST_CVR	32	0	rw	Address 0xe000e018
SYST_CALIB	32	0	rw	Address 0xe000e01c
NVIC_ISER0	32	0	rw	Address 0xe000e100
NVIC_ICER0	32	0	rw	Address 0xe000e180
NVIC_ISPR0	32	0	rw	Address 0xe000e200
NVIC_ICPR0	32	0	rw	Address 0xe000e280
NVIC_IPR0	32	0	rw	Address 0xe000e400
NVIC_IPR1	32	0	rw	Address 0xe000e404
NVIC_IPR2	32	0	rw	Address 0xe000e408
NVIC_IPR3	32	0	rw	Address 0xe000e40c
CPUID	32	410cc601	r-	Address 0xe000ed00
ICSR	32	1000	rw	Address 0xe000ed04
VTOR	32	0	rw	Address 0xe000ed08
AIRCR	32	fa050000	rw	Address 0xe000ed0c
SCR	32	0	rw	Address 0xe000ed10
CCR	32	200	rw	Address 0xe000ed14
SHPR2	32	0	rw	Address 0xe000ed1c
SHPR3	32	0	rw	Address 0xe000ed20
SHCSR	32	0	rw	Address 0xe000ed24
MPU_RNR	32	0	rw	Address 0xe000ed98
MPU_RBAR	32	0	rw	Address 0xe000ed9c
MPU_RASR	32	0	rw	Address 0xe000eda0
MPU_RBAR_A1	32	0	rw	Address 0xe000eda4
MPU_RASR_A1	32	0	rw	Address 0xe000eda8
MPU_RBAR_A2	32	0	rw	Address 0xe000edac
MPU_RASR_A2	32	0	rw	Address 0xe000edb0
MPU_RBAR_A3	32	0	rw	Address 0xe000edb4
MPU_RASR_A3	32	0	rw	Address 0xe000edb8

Table 13.3: Registers at level 1, group:System

13.1.4 Integration_support

Registers at level:1, group:Integration_support

Name	Bits	Initial-Hex	RW	Description
executionPri	32	7fffffff	r-	current execution priority level
stackDomain	32	8ea5818	r-	stack domain for current execution level

Table 13.4: Registers at level 1, group:Integration_support