OVP Guide to Using Processor Models

Model Specific Information for variant MIPS32_1004Kc

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Table of Contents

1 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS32 Configurable Processor Model

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.
Cache model does not implement coherency

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

MIPS32 Instruction set implemented
MMU Type: Standard TLB
L1 I and D cache model in either full or tag-only mode implemented (disabled by default)
Vectored interrupts implemented
MIPS16e ASE implemented
MT ASE implemented
DSP ASE implemented

2 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
    mips.ovpworld.org/processor/mips32/1.0

2.2 GDB Path

The default GDB for this model is found at:
    $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/mips-sde-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
    mips.ovpworld.org/semihosting/mips32SDE/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code
The ELF code supported by this model is: 0x8

3 Other Variants in this Model

Table 1.

Variant
ISA
M14K
M14KcTLB
M14KcFMM
4KEc
4KEm
4KEp
M4K
4Kc
4Km
4Kp
24Kc
24Kf
24KEc
24KEf
34Kc
34Kf
34Kn
74Kc
74Kf
1004Kc
1004Kf
1074Kc
1074Kf
microAptivC
microAptivP
microAptivCF
interAptiv
interAptivUP
proAptiv

4 Bus Ports

Table 2.

Type	Name	min	max
master (initiator)	INSTRUCTION	10	36
master (initiator)	DATA	10	36

5 Net Ports

Table 3.

Name	Type	Description
reset	input	CMP reset
dint	input	Debug external interrupt
int0	input	GIC external interrupt
int1	input	GIC external interrupt
int2	input	GIC external interrupt
int3	input	GIC external interrupt
int4	input	GIC external interrupt
int5	input	GIC external interrupt
int6	input	GIC external interrupt
int7	input	GIC external interrupt
int8	input	GIC external interrupt
int9	input	GIC external interrupt
int10	input	GIC external interrupt
int11	input	GIC external interrupt
int12	input	GIC external interrupt
int13	input	GIC external interrupt
int14	input	GIC external interrupt
int15	input	GIC external interrupt
int16	input	GIC external interrupt
int17	input	GIC external interrupt
int18	input	GIC external interrupt
int19	input	GIC external interrupt
int20	input	GIC external interrupt
int21	input	GIC external interrupt
int22	input	GIC external interrupt
int23	input	GIC external interrupt
int24	input	GIC external interrupt
int25	input	GIC external interrupt
int26	input	GIC external interrupt
int27	input	GIC external interrupt
int28	input	GIC external interrupt
int29	input	GIC external interrupt
int30	input	GIC external interrupt
int31	input	GIC external interrupt
int32	input	GIC external interrupt
int33	input	GIC external interrupt
int34	input	GIC external interrupt
int35	input	GIC external interrupt

int36	input	GIC external interrupt
int37	input	GIC external interrupt
int38	input	GIC external interrupt
int39	input	GIC external interrupt
yq_CPU0	input	Yield qualifier
yq0_CPU0	input	Yield qualifier
yq1_CPU0	input	Yield qualifier
yq2_CPU0	input	Yield qualifier
yq3_CPU0	input	Yield qualifier
yq4_CPU0	input	Yield qualifier
yq5_CPU0	input	Yield qualifier
yq6_CPU0	input	Yield qualifier
yq7_CPU0	input	Yield qualifier
yq8_CPU0	input	Yield qualifier
yq9_CPU0	input	Yield qualifier
yq10_CPU0	input	Yield qualifier
yq11_CPU0	input	Yield qualifier
yq12_CPU0	input	Yield qualifier
yq13_CPU0	input	Yield qualifier
yq14_CPU0	input	Yield qualifier
yq15_CPU0	input	Yield qualifier
hwint0_CPU0_VPE0	input	External interrupt
hwint1_CPU0_VPE0	input	External interrupt
hwint2_CPU0_VPE0	input	External interrupt
hwint3_CPU0_VPE0	input	External interrupt
hwint4_CPU0_VPE0	input	External interrupt
hwint5_CPU0_VPE0	input	External interrupt
nmi_CPU0_VPE0	input	Non-maskable external interrupt
hwint0	input	External interrupt for compatibility
hwint0_CPU0_VPE1	input	External interrupt
hwint1_CPU0_VPE1	input	External interrupt
hwint2_CPU0_VPE1	input	External interrupt
hwint3_CPU0_VPE1	input	External interrupt
hwint4_CPU0_VPE1	input	External interrupt
hwint5_CPU0_VPE1	input	External interrupt
nmi_CPU0_VPE1	input	Non-maskable external interrupt
yq_CPU1	input	Yield qualifier
yq0_CPU1	input	Yield qualifier
yq1_CPU1	input	Yield qualifier
yq2_CPU1	input	Yield qualifier
yq3_CPU1	input	Yield qualifier
yq4_CPU1	input	Yield qualifier

yq5_CPU1	input	Yield qualifier
yq6_CPU1	input	Yield qualifier
yq7_CPU1	input	Yield qualifier
yq8_CPU1	input	Yield qualifier
yq9_CPU1	input	Yield qualifier
yq10_CPU1	input	Yield qualifier
yq11_CPU1	input	Yield qualifier
yq12_CPU1	input	Yield qualifier
yq13_CPU1	input	Yield qualifier
yq14_CPU1	input	Yield qualifier
yq15_CPU1	input	Yield qualifier
hwint0_CPU1_VPE0	input	External interrupt
hwint1_CPU1_VPE0	input	External interrupt
hwint2_CPU1_VPE0	input	External interrupt
hwint3_CPU1_VPE0	input	External interrupt
hwint4_CPU1_VPE0	input	External interrupt
hwint5_CPU1_VPE0	input	External interrupt
nmi_CPU1_VPE0	input	Non-maskable external interrupt
hwint0_CPU1_VPE1	input	External interrupt
hwint1_CPU1_VPE1	input	External interrupt
hwint2_CPU1_VPE1	input	External interrupt
hwint3_CPU1_VPE1	input	External interrupt
hwint4_CPU1_VPE1	input	External interrupt
hwint5_CPU1_VPE1	input	External interrupt
nmi_CPU1_VPE1	input	Non-maskable external interrupt
yq_CPU2	input	Yield qualifier
yq0_CPU2	input	Yield qualifier
yq1_CPU2	input	Yield qualifier
yq2_CPU2	input	Yield qualifier
yq3_CPU2	input	Yield qualifier
yq4_CPU2	input	Yield qualifier
yq5_CPU2	input	Yield qualifier
yq6_CPU2	input	Yield qualifier
yq7_CPU2	input	Yield qualifier
yq8_CPU2	input	Yield qualifier
yq9_CPU2	input	Yield qualifier
yq10_CPU2	input	Yield qualifier
yq11_CPU2	input	Yield qualifier
yq12_CPU2	input	Yield qualifier
yq13_CPU2	input	Yield qualifier
yq14_CPU2	input	Yield qualifier
yq15_CPU2	input	Yield qualifier

hwint0_CPU2_VPE0	input	External interrupt
hwint1_CPU2_VPE0	input	External interrupt
hwint2_CPU2_VPE0	input	External interrupt
hwint3_CPU2_VPE0	input	External interrupt
hwint4_CPU2_VPE0	input	External interrupt
hwint5_CPU2_VPE0	input	External interrupt
nmi_CPU2_VPE0	input	Non-maskable external interrupt
hwint0_CPU2_VPE1	input	External interrupt
hwint1_CPU2_VPE1	input	External interrupt
hwint2_CPU2_VPE1	input	External interrupt
hwint3_CPU2_VPE1	input	External interrupt
hwint4_CPU2_VPE1	input	External interrupt
hwint5_CPU2_VPE1	input	External interrupt
nmi_CPU2_VPE1	input	Non-maskable external interrupt
yq_CPU3	input	Yield qualifier
yq0_CPU3	input	Yield qualifier
yq1_CPU3	input	Yield qualifier
yq2_CPU3	input	Yield qualifier
yq3_CPU3	input	Yield qualifier
yq4_CPU3	input	Yield qualifier
yq5_CPU3	input	Yield qualifier
yq6_CPU3	input	Yield qualifier
yq7_CPU3	input	Yield qualifier
yq8_CPU3	input	Yield qualifier
yq9_CPU3	input	Yield qualifier
yq10_CPU3	input	Yield qualifier
yq11_CPU3	input	Yield qualifier
yq12_CPU3	input	Yield qualifier
yq13_CPU3	input	Yield qualifier
yq14_CPU3	input	Yield qualifier
yq15_CPU3	input	Yield qualifier
hwint0_CPU3_VPE0	input	External interrupt
hwint1_CPU3_VPE0	input	External interrupt
hwint2_CPU3_VPE0	input	External interrupt
hwint3_CPU3_VPE0	input	External interrupt
hwint4_CPU3_VPE0	input	External interrupt
hwint5_CPU3_VPE0	input	External interrupt
nmi_CPU3_VPE0	input	Non-maskable external interrupt
hwint0_CPU3_VPE1	input	External interrupt
hwint1_CPU3_VPE1	input	External interrupt
hwint2_CPU3_VPE1	input	External interrupt
hwint3_CPU3_VPE1	input	External interrupt

hwint4_CPU3_VPE1	input	External interrupt
hwint5_CPU3_VPE1	input	External interrupt
nmi_CPU3_VPE1	input	Non-maskable external interrupt

6 FIFO Ports

No FIFO Ports in this model.

7 Parameters

Table 4.

Name	Type	Description
cacheenable	Enumeration	Select cache model mode default=0 tag=1 full=2
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)

supportDenormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentControl_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentControl_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentControl_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentControl_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentControl_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentControl_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentControl_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentControl_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentControl_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 register
mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
statusFR	Boolean	Override power on value in Status.FR (Floating point register mode)

configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT
configSB	Boolean	Override Config.SB (simple bus transfers only)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Dcache associativity)
config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config1FP	Boolean	Override Config1.FP (FPU present)
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC

config3ULRI	Boolean	Override Config3.ULRI
externalinterrupt	Boolean	Override Config3.VEIC (enables the use of an external interrupt controller)
vectoredinterrupt	Boolean	Override Config3.VInt (enables vectored interrupts)
config3VZ	Boolean	Override Config3.VZ
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5NFExists	Boolean	Override Config5.NFExists
config5MSAEn	Boolean	Override Config5.MSAEn
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE
config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/ SNaN encodings match IEEE 754-2008 recommendation)
firPS	Boolean	Override FIR.PS (PS floating point type implemented)
firHas2008	Boolean	Override FIR.Has2008 (one or more IEEE 754-2008 features present)
intctlIPFDC	Uns32	Override IntCtl.IPFDC
intctlIPTI	Uns32	Override IntCtl.IPTI
pridRevision	Uns32	Override PRId.Revision
srsctlHSS	Uns32	Override SRSCtl.HSS (number of shadow register sets)
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
firstBEVExceptionBaseMaskBit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE.BEVExceptionBaseMask field. Only used when SegCtl present

EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPES
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY

CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0. Only used when SegCtl present
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1. Only used when SegCtl present
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2. Only used when SegCtl present
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3. Only used when SegCtl present
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ISPRAM size in bytes>) - 11)
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<DSPRAM size in bytes>) - 11)
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset)

8 Execution Modes

Table 5.

Name	Code
KERNEL	0
DEBUG	1
SUPERVISOR	2
USER	3

9 Exceptions

Table 6.

Name	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Bp	9
RI	10
CpU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
Prot	29
CacheErr	30

10 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1: CMP

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has 4 children:

CPU0, CPU1, CPU2 and CPU3

10.2 Level 2: CPU

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has 2 children:

CPU0_VPE0 and CPU0_VPE1

10.3 Level 3: VPE

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has 4 register groups:

Table 7.

Group name	Registers
COP0	50
CMP_GCR	27
CMP_CPC	11
CMP_GIC	746

This level in the model hierarchy has one child:

CPU0_TC0

10.4 Level 4: TC

This level in the model hierarchy has 16 commands.

This level in the model hierarchy has 7 register groups:

Table 8.

Group name	Registers
Core	33
DSP	9
COP0	64
CMP_GCR	27
CMP_CPC	11
CMP_GIC	746
Integration_support	1

This level in the model hierarchy has no children.

11 Model Commands

11.1 Level 1: CMP

Table 9.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

11.2 Level 2: CPU

Table 10.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

11.3 Level 3: VPE

Table 11.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing

11.4 Level 4: TC

Table 12.

Name	Arguments
isync	specify instruction address range for synchronous execution
itrace	enable or disable instruction tracing
mipsCOP0	<register> <select>
mipsCacheDisable	
mipsCacheEnable	-tag|-full
mipsCacheRatio	-icache|-dcache
mipsCacheReport	
mipsCacheReset	
mipsCacheTrace	-on|-off [-nocached|-nouncached] [-noicache|-nodcache] [-noartifact|-notrue]
mipsDebugFlags	<value>
mipsReadRegister	<resource> <offset>
mipsReadTLBEntry	<index>
mipsTLBDump	
mipsTLBGetPhys	<virtual address> <ASID>
mipsWriteRegister	<resource> <offset> <value>
mipsWriteTLBEntry	<index> <lo0> <lo1> <hi0> <mask>

12 Registers

12.1 Level 1: CMP

No registers.

12.2 Level 2: CPU

No registers.

12.3 Level 3: VPE

12.3.1 COP0

Table 13.

Name	Bits	Initial value (Hex)		Description
bad	32	0	rw	CP0 register 8/0 (badvaaddr)
cause	32	0	rw	CP0 register 13/0 (cause)
index	32	0	rw	CP0 register 0/0
mvpcontrol	32	0	rw	CP0 register 0/1
mvpconf0	32	88008401	rw	CP0 register 0/2
mvpconf1	32	0	rw	CP0 register 0/3
random	32	0	rw	CP0 register 1/0
vpecontrol	32	0	rw	CP0 register 1/1
vpeconf0	32	80000003	rw	CP0 register 1/2
vpeconf1	32	0	rw	CP0 register 1/3
yqmask	32	0	rw	CP0 register 1/4
vpeschedule	32	0	rw	CP0 register 1/5
vpeschefback	32	0	rw	CP0 register 1/6
vpeopt	32	0	rw	CP0 register 1/7
entrylo0	32	0	rw	CP0 register 2/0
entrylo1	32	0	rw	CP0 register 3/0
context	32	0	rw	CP0 register 4/0
pagemask	32	0	rw	CP0 register 5/0
wired	32	0	rw	CP0 register 6/0
srsconf0	32	3fffffff	rw	CP0 register 6/1
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
count	32	0	rw	CP0 register 9/0
compare	32	0	rw	CP0 register 11/0
intctl	32	e0000000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
epc	32	0	rw	CP0 register 14/0
prid	32	19900	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
cmgcrbase	32	1fbf800	rw	CP0 register 15/3
config	32	80048482	rw	CP0 register 16/0
config1	32	9e231186	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2

config3	32	20002424	rw	CP0 register 16/3
config7	32	80080100	rw	CP0 register 16/7
depc	32	0	rw	CP0 register 24/0
errctl	32	0	rw	CP0 register 26/0
itaglo	32	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	32	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
dtaghi	32	0	rw	CP0 register 29/2
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0

12.3.2 CMP_GCR

Table 14.

Name	Bits	Initial value (Hex)		Description
GCR_CONFIG	32	3	r-	
GCR_BASE	32	1fbf8000	rw	
GCR_CONTROL	32	10001	rw	
GCR_ACCESS	32	ff	rw	
GCR_REV	32	0	r-	
GCR_ERROR_MASK	32	0	rw	
GCR_ERROR_CAUSE	32	0	rw	
GCR_ERROR_ADDR	32	0	rw	
GCR_ERROR_MULT	32	0	rw	
GCR_GIC_BASE	32	0	rw	
GCR_CPC_BASE	32	0	rw	
GCR_GIC_STATUS	32	1	r-	
GCR_CACHE_REV	32	0	r-	
GCR_CPC_STATUS	32	1	r-	
GCR_IOCU1_REV	32	0	r-	
GCR_CL_RESET_RELEASE_L	32	0	-w	
GCR_CL_COHERENCE_L	32	0	rw	
GCR_CL_CONFIG_L	32	1	r-	
GCR_CL_OTHER_L	32	0	rw	
GCR_CL_RESET_BASE_L	32	bfc00000	rw	
GCR_CL_ID_L	32	0	r-	

GCR_CL_RESET_RELEASE_O	32	0	-w	
GCR_CL_COHERENCE_O	32	0	rw	
GCR_CL_CONFIG_O	32	1	r-	
GCR_CL_OTHER_O	32	0	rw	
GCR_CL_RESET_BASE_O	32	bfc00000	rw	
GCR_CL_ID_O	32	0	r-	

12.3.3 CMP_CPC

Table 15.

Name	Bits	Initial value (Hex)		Description
CPC_ACCESS	32	ff	rw	
CPC_SEQDEL	32	0	rw	
CPC_RAIL	32	0	rw	
CPC_RESETLEN	32	0	rw	
CPC_REVISION	32	0	r-	
CPC_CMD_L	32	0	rw	
CPC_STAT_CONF_L	32	380200	rw	
CPC_OTHER_L	32	0	rw	
CPC_CMD_O	32	0	rw	
CPC_STAT_CONF_O	32	380200	rw	
CPC_OTHER_O	32	0	rw	

12.3.4 CMP_GIC

Table 16.

Name	Bits	Initial value (Hex)		Description
GIC_SH_CONFIG	32	8040007	rw	
GIC_CounterLo	32	0	rw	
GIC_CounterHi	32	0	rw	
GIC_SH_REVISION	32	0	r-	
GIC_SH_POL31_0	32	0	rw	
GIC_SH_POL63_32	32	0	rw	
GIC_SH_POL95_64	32	0	rw	
GIC_SH_POL127_96	32	0	rw	
GIC_SH_POL159_128	32	0	rw	
GIC_SH_POL191_160	32	0	rw	
GIC_SH_POL223_192	32	0	rw	
GIC_SH_POL255_224	32	0	rw	
GIC_SH_TRIG31_0	32	0	rw	
GIC_SH_TRIG63_32	32	0	rw	
GIC_SH_TRIG95_64	32	0	rw	

GIC_SH_TRIG127_96	32	0	rw	
GIC_SH_TRIG159_128	32	0	rw	
GIC_SH_TRIG191_160	32	0	rw	
GIC_SH_TRIG223_192	32	0	rw	
GIC_SH_TRIG255_224	32	0	rw	
GIC_SH_DUAL31_0	32	0	rw	
GIC_SH_DUAL63_32	32	0	rw	
GIC_SH_DUAL95_64	32	0	rw	
GIC_SH_DUAL127_96	32	0	rw	
GIC_SH_DUAL159_128	32	0	rw	
GIC_SH_DUAL191_160	32	0	rw	
GIC_SH_DUAL223_192	32	0	rw	
GIC_SH_DUAL255_224	32	0	rw	
GIC_SH_WEDGE	32	0	-w	
GIC_SH_RMASK31_0	32	0	-w	
GIC_SH_RMASK63_32	32	0	-w	
GIC_SH_RMASK95_64	32	0	-w	
GIC_SH_RMASK127_96	32	0	-w	
GIC_SH_RMASK159_128	32	0	-w	
GIC_SH_RMASK191_160	32	0	-w	
GIC_SH_RMASK223_192	32	0	-w	
GIC_SH_RMASK255_224	32	0	-w	
GIC_SH_SMASK31_0	32	0	-w	
GIC_SH_SMASK63_32	32	0	-w	
GIC_SH_SMASK95_64	32	0	-w	
GIC_SH_SMASK127_96	32	0	-w	
GIC_SH_SMASK159_128	32	0	-w	
GIC_SH_SMASK191_160	32	0	-w	
GIC_SH_SMASK223_192	32	0	-w	
GIC_SH_SMASK255_224	32	0	-w	
GIC_SH_MASK31_0	32	0	r-	
GIC_SH_MASK63_32	32	0	r-	
GIC_SH_MASK95_64	32	0	r-	
GIC_SH_MASK127_96	32	0	r-	
GIC_SH_MASK159_128	32	0	r-	
GIC_SH_MASK191_160	32	0	r-	
GIC_SH_MASK223_192	32	0	r-	
GIC_SH_MASK255_224	32	0	r-	
GIC_SH_PEND31_0	32	0	r-	
GIC_SH_PEND63_32	32	0	r-	
GIC_SH_PEND95_64	32	0	r-	
GIC_SH_PEND127_96	32	0	r-	

GIC_SH_PEND159_128	32	0	r-	
GIC_SH_PEND191_160	32	0	r-	
GIC_SH_PEND223_192	32	0	r-	
GIC_SH_PEND255_224	32	0	r-	
GIC_SH_MAP000_PIN	32	80000000	rw	
GIC_SH_MAP001_PIN	32	80000000	rw	
GIC_SH_MAP002_PIN	32	80000000	rw	
GIC_SH_MAP003_PIN	32	80000000	rw	
GIC_SH_MAP004_PIN	32	80000000	rw	
GIC_SH_MAP005_PIN	32	80000000	rw	
GIC_SH_MAP006_PIN	32	80000000	rw	
GIC_SH_MAP007_PIN	32	80000000	rw	
GIC_SH_MAP008_PIN	32	80000000	rw	
GIC_SH_MAP009_PIN	32	80000000	rw	
GIC_SH_MAP010_PIN	32	80000000	rw	
GIC_SH_MAP011_PIN	32	80000000	rw	
GIC_SH_MAP012_PIN	32	80000000	rw	
GIC_SH_MAP013_PIN	32	80000000	rw	
GIC_SH_MAP014_PIN	32	80000000	rw	
GIC_SH_MAP015_PIN	32	80000000	rw	
GIC_SH_MAP016_PIN	32	80000000	rw	
GIC_SH_MAP017_PIN	32	80000000	rw	
GIC_SH_MAP018_PIN	32	80000000	rw	
GIC_SH_MAP019_PIN	32	80000000	rw	
GIC_SH_MAP020_PIN	32	80000000	rw	
GIC_SH_MAP021_PIN	32	80000000	rw	
GIC_SH_MAP022_PIN	32	80000000	rw	
GIC_SH_MAP023_PIN	32	80000000	rw	
GIC_SH_MAP024_PIN	32	80000000	rw	
GIC_SH_MAP025_PIN	32	80000000	rw	
GIC_SH_MAP026_PIN	32	80000000	rw	
GIC_SH_MAP027_PIN	32	80000000	rw	
GIC_SH_MAP028_PIN	32	80000000	rw	
GIC_SH_MAP029_PIN	32	80000000	rw	
GIC_SH_MAP030_PIN	32	80000000	rw	
GIC_SH_MAP031_PIN	32	80000000	rw	
GIC_SH_MAP032_PIN	32	80000000	rw	
GIC_SH_MAP033_PIN	32	80000000	rw	
GIC_SH_MAP034_PIN	32	80000000	rw	
GIC_SH_MAP035_PIN	32	80000000	rw	
GIC_SH_MAP036_PIN	32	80000000	rw	
GIC_SH_MAP037_PIN	32	80000000	rw	

GIC_SH_MAP038_PIN	32	80000000	rw	
GIC_SH_MAP039_PIN	32	80000000	rw	
GIC_SH_MAP040_PIN	32	80000000	rw	
GIC_SH_MAP041_PIN	32	80000000	rw	
GIC_SH_MAP042_PIN	32	80000000	rw	
GIC_SH_MAP043_PIN	32	80000000	rw	
GIC_SH_MAP044_PIN	32	80000000	rw	
GIC_SH_MAP045_PIN	32	80000000	rw	
GIC_SH_MAP046_PIN	32	80000000	rw	
GIC_SH_MAP047_PIN	32	80000000	rw	
GIC_SH_MAP048_PIN	32	80000000	rw	
GIC_SH_MAP049_PIN	32	80000000	rw	
GIC_SH_MAP050_PIN	32	80000000	rw	
GIC_SH_MAP051_PIN	32	80000000	rw	
GIC_SH_MAP052_PIN	32	80000000	rw	
GIC_SH_MAP053_PIN	32	80000000	rw	
GIC_SH_MAP054_PIN	32	80000000	rw	
GIC_SH_MAP055_PIN	32	80000000	rw	
GIC_SH_MAP056_PIN	32	80000000	rw	
GIC_SH_MAP057_PIN	32	80000000	rw	
GIC_SH_MAP058_PIN	32	80000000	rw	
GIC_SH_MAP059_PIN	32	80000000	rw	
GIC_SH_MAP060_PIN	32	80000000	rw	
GIC_SH_MAP061_PIN	32	80000000	rw	
GIC_SH_MAP062_PIN	32	80000000	rw	
GIC_SH_MAP063_PIN	32	80000000	rw	
GIC_SH_MAP064_PIN	32	80000000	rw	
GIC_SH_MAP065_PIN	32	80000000	rw	
GIC_SH_MAP066_PIN	32	80000000	rw	
GIC_SH_MAP067_PIN	32	80000000	rw	
GIC_SH_MAP068_PIN	32	80000000	rw	
GIC_SH_MAP069_PIN	32	80000000	rw	
GIC_SH_MAP070_PIN	32	80000000	rw	
GIC_SH_MAP071_PIN	32	80000000	rw	
GIC_SH_MAP072_PIN	32	80000000	rw	
GIC_SH_MAP073_PIN	32	80000000	rw	
GIC_SH_MAP074_PIN	32	80000000	rw	
GIC_SH_MAP075_PIN	32	80000000	rw	
GIC_SH_MAP076_PIN	32	80000000	rw	
GIC_SH_MAP077_PIN	32	80000000	rw	
GIC_SH_MAP078_PIN	32	80000000	rw	
GIC_SH_MAP079_PIN	32	80000000	rw	

GIC_SH_MAP080_PIN	32	80000000	rw	
GIC_SH_MAP081_PIN	32	80000000	rw	
GIC_SH_MAP082_PIN	32	80000000	rw	
GIC_SH_MAP083_PIN	32	80000000	rw	
GIC_SH_MAP084_PIN	32	80000000	rw	
GIC_SH_MAP085_PIN	32	80000000	rw	
GIC_SH_MAP086_PIN	32	80000000	rw	
GIC_SH_MAP087_PIN	32	80000000	rw	
GIC_SH_MAP088_PIN	32	80000000	rw	
GIC_SH_MAP089_PIN	32	80000000	rw	
GIC_SH_MAP090_PIN	32	80000000	rw	
GIC_SH_MAP091_PIN	32	80000000	rw	
GIC_SH_MAP092_PIN	32	80000000	rw	
GIC_SH_MAP093_PIN	32	80000000	rw	
GIC_SH_MAP094_PIN	32	80000000	rw	
GIC_SH_MAP095_PIN	32	80000000	rw	
GIC_SH_MAP096_PIN	32	80000000	rw	
GIC_SH_MAP097_PIN	32	80000000	rw	
GIC_SH_MAP098_PIN	32	80000000	rw	
GIC_SH_MAP099_PIN	32	80000000	rw	
GIC_SH_MAP100_PIN	32	80000000	rw	
GIC_SH_MAP101_PIN	32	80000000	rw	
GIC_SH_MAP102_PIN	32	80000000	rw	
GIC_SH_MAP103_PIN	32	80000000	rw	
GIC_SH_MAP104_PIN	32	80000000	rw	
GIC_SH_MAP105_PIN	32	80000000	rw	
GIC_SH_MAP106_PIN	32	80000000	rw	
GIC_SH_MAP107_PIN	32	80000000	rw	
GIC_SH_MAP108_PIN	32	80000000	rw	
GIC_SH_MAP109_PIN	32	80000000	rw	
GIC_SH_MAP110_PIN	32	80000000	rw	
GIC_SH_MAP111_PIN	32	80000000	rw	
GIC_SH_MAP112_PIN	32	80000000	rw	
GIC_SH_MAP113_PIN	32	80000000	rw	
GIC_SH_MAP114_PIN	32	80000000	rw	
GIC_SH_MAP115_PIN	32	80000000	rw	
GIC_SH_MAP116_PIN	32	80000000	rw	
GIC_SH_MAP117_PIN	32	80000000	rw	
GIC_SH_MAP118_PIN	32	80000000	rw	
GIC_SH_MAP119_PIN	32	80000000	rw	
GIC_SH_MAP120_PIN	32	80000000	rw	
GIC_SH_MAP121_PIN	32	80000000	rw	

GIC_SH_MAP122_PIN	32	80000000	rw	
GIC_SH_MAP123_PIN	32	80000000	rw	
GIC_SH_MAP124_PIN	32	80000000	rw	
GIC_SH_MAP125_PIN	32	80000000	rw	
GIC_SH_MAP126_PIN	32	80000000	rw	
GIC_SH_MAP127_PIN	32	80000000	rw	
GIC_SH_MAP128_PIN	32	80000000	rw	
GIC_SH_MAP129_PIN	32	80000000	rw	
GIC_SH_MAP130_PIN	32	80000000	rw	
GIC_SH_MAP131_PIN	32	80000000	rw	
GIC_SH_MAP132_PIN	32	80000000	rw	
GIC_SH_MAP133_PIN	32	80000000	rw	
GIC_SH_MAP134_PIN	32	80000000	rw	
GIC_SH_MAP135_PIN	32	80000000	rw	
GIC_SH_MAP136_PIN	32	80000000	rw	
GIC_SH_MAP137_PIN	32	80000000	rw	
GIC_SH_MAP138_PIN	32	80000000	rw	
GIC_SH_MAP139_PIN	32	80000000	rw	
GIC_SH_MAP140_PIN	32	80000000	rw	
GIC_SH_MAP141_PIN	32	80000000	rw	
GIC_SH_MAP142_PIN	32	80000000	rw	
GIC_SH_MAP143_PIN	32	80000000	rw	
GIC_SH_MAP144_PIN	32	80000000	rw	
GIC_SH_MAP145_PIN	32	80000000	rw	
GIC_SH_MAP146_PIN	32	80000000	rw	
GIC_SH_MAP147_PIN	32	80000000	rw	
GIC_SH_MAP148_PIN	32	80000000	rw	
GIC_SH_MAP149_PIN	32	80000000	rw	
GIC_SH_MAP150_PIN	32	80000000	rw	
GIC_SH_MAP151_PIN	32	80000000	rw	
GIC_SH_MAP152_PIN	32	80000000	rw	
GIC_SH_MAP153_PIN	32	80000000	rw	
GIC_SH_MAP154_PIN	32	80000000	rw	
GIC_SH_MAP155_PIN	32	80000000	rw	
GIC_SH_MAP156_PIN	32	80000000	rw	
GIC_SH_MAP157_PIN	32	80000000	rw	
GIC_SH_MAP158_PIN	32	80000000	rw	
GIC_SH_MAP159_PIN	32	80000000	rw	
GIC_SH_MAP160_PIN	32	80000000	rw	
GIC_SH_MAP161_PIN	32	80000000	rw	
GIC_SH_MAP162_PIN	32	80000000	rw	
GIC_SH_MAP163_PIN	32	80000000	rw	

GIC_SH_MAP164_PIN	32	80000000	rw	
GIC_SH_MAP165_PIN	32	80000000	rw	
GIC_SH_MAP166_PIN	32	80000000	rw	
GIC_SH_MAP167_PIN	32	80000000	rw	
GIC_SH_MAP168_PIN	32	80000000	rw	
GIC_SH_MAP169_PIN	32	80000000	rw	
GIC_SH_MAP170_PIN	32	80000000	rw	
GIC_SH_MAP171_PIN	32	80000000	rw	
GIC_SH_MAP172_PIN	32	80000000	rw	
GIC_SH_MAP173_PIN	32	80000000	rw	
GIC_SH_MAP174_PIN	32	80000000	rw	
GIC_SH_MAP175_PIN	32	80000000	rw	
GIC_SH_MAP176_PIN	32	80000000	rw	
GIC_SH_MAP177_PIN	32	80000000	rw	
GIC_SH_MAP178_PIN	32	80000000	rw	
GIC_SH_MAP179_PIN	32	80000000	rw	
GIC_SH_MAP180_PIN	32	80000000	rw	
GIC_SH_MAP181_PIN	32	80000000	rw	
GIC_SH_MAP182_PIN	32	80000000	rw	
GIC_SH_MAP183_PIN	32	80000000	rw	
GIC_SH_MAP184_PIN	32	80000000	rw	
GIC_SH_MAP185_PIN	32	80000000	rw	
GIC_SH_MAP186_PIN	32	80000000	rw	
GIC_SH_MAP187_PIN	32	80000000	rw	
GIC_SH_MAP188_PIN	32	80000000	rw	
GIC_SH_MAP189_PIN	32	80000000	rw	
GIC_SH_MAP190_PIN	32	80000000	rw	
GIC_SH_MAP191_PIN	32	80000000	rw	
GIC_SH_MAP192_PIN	32	80000000	rw	
GIC_SH_MAP193_PIN	32	80000000	rw	
GIC_SH_MAP194_PIN	32	80000000	rw	
GIC_SH_MAP195_PIN	32	80000000	rw	
GIC_SH_MAP196_PIN	32	80000000	rw	
GIC_SH_MAP197_PIN	32	80000000	rw	
GIC_SH_MAP198_PIN	32	80000000	rw	
GIC_SH_MAP199_PIN	32	80000000	rw	
GIC_SH_MAP200_PIN	32	80000000	rw	
GIC_SH_MAP201_PIN	32	80000000	rw	
GIC_SH_MAP202_PIN	32	80000000	rw	
GIC_SH_MAP203_PIN	32	80000000	rw	
GIC_SH_MAP204_PIN	32	80000000	rw	
GIC_SH_MAP205_PIN	32	80000000	rw	

GIC_SH_MAP206_PIN	32	80000000	rw	
GIC_SH_MAP207_PIN	32	80000000	rw	
GIC_SH_MAP208_PIN	32	80000000	rw	
GIC_SH_MAP209_PIN	32	80000000	rw	
GIC_SH_MAP210_PIN	32	80000000	rw	
GIC_SH_MAP211_PIN	32	80000000	rw	
GIC_SH_MAP212_PIN	32	80000000	rw	
GIC_SH_MAP213_PIN	32	80000000	rw	
GIC_SH_MAP214_PIN	32	80000000	rw	
GIC_SH_MAP215_PIN	32	80000000	rw	
GIC_SH_MAP216_PIN	32	80000000	rw	
GIC_SH_MAP217_PIN	32	80000000	rw	
GIC_SH_MAP218_PIN	32	80000000	rw	
GIC_SH_MAP219_PIN	32	80000000	rw	
GIC_SH_MAP220_PIN	32	80000000	rw	
GIC_SH_MAP221_PIN	32	80000000	rw	
GIC_SH_MAP222_PIN	32	80000000	rw	
GIC_SH_MAP223_PIN	32	80000000	rw	
GIC_SH_MAP224_PIN	32	80000000	rw	
GIC_SH_MAP225_PIN	32	80000000	rw	
GIC_SH_MAP226_PIN	32	80000000	rw	
GIC_SH_MAP227_PIN	32	80000000	rw	
GIC_SH_MAP228_PIN	32	80000000	rw	
GIC_SH_MAP229_PIN	32	80000000	rw	
GIC_SH_MAP230_PIN	32	80000000	rw	
GIC_SH_MAP231_PIN	32	80000000	rw	
GIC_SH_MAP232_PIN	32	80000000	rw	
GIC_SH_MAP233_PIN	32	80000000	rw	
GIC_SH_MAP234_PIN	32	80000000	rw	
GIC_SH_MAP235_PIN	32	80000000	rw	
GIC_SH_MAP236_PIN	32	80000000	rw	
GIC_SH_MAP237_PIN	32	80000000	rw	
GIC_SH_MAP238_PIN	32	80000000	rw	
GIC_SH_MAP239_PIN	32	80000000	rw	
GIC_SH_MAP240_PIN	32	80000000	rw	
GIC_SH_MAP241_PIN	32	80000000	rw	
GIC_SH_MAP242_PIN	32	80000000	rw	
GIC_SH_MAP243_PIN	32	80000000	rw	
GIC_SH_MAP244_PIN	32	80000000	rw	
GIC_SH_MAP245_PIN	32	80000000	rw	
GIC_SH_MAP246_PIN	32	80000000	rw	
GIC_SH_MAP247_PIN	32	80000000	rw	

GIC_SH_MAP248_PIN	32	80000000	rw	
GIC_SH_MAP249_PIN	32	80000000	rw	
GIC_SH_MAP250_PIN	32	80000000	rw	
GIC_SH_MAP251_PIN	32	80000000	rw	
GIC_SH_MAP252_PIN	32	80000000	rw	
GIC_SH_MAP253_PIN	32	80000000	rw	
GIC_SH_MAP254_PIN	32	80000000	rw	
GIC_SH_MAP255_PIN	32	80000000	rw	
GIC_SH_MAP000_VPE31_0	32	0	rw	
GIC_SH_MAP001_VPE31_0	32	0	rw	
GIC_SH_MAP002_VPE31_0	32	0	rw	
GIC_SH_MAP003_VPE31_0	32	0	rw	
GIC_SH_MAP004_VPE31_0	32	0	rw	
GIC_SH_MAP005_VPE31_0	32	0	rw	
GIC_SH_MAP006_VPE31_0	32	0	rw	
GIC_SH_MAP007_VPE31_0	32	0	rw	
GIC_SH_MAP008_VPE31_0	32	0	rw	
GIC_SH_MAP009_VPE31_0	32	0	rw	
GIC_SH_MAP010_VPE31_0	32	0	rw	
GIC_SH_MAP011_VPE31_0	32	0	rw	
GIC_SH_MAP012_VPE31_0	32	0	rw	
GIC_SH_MAP013_VPE31_0	32	0	rw	
GIC_SH_MAP014_VPE31_0	32	0	rw	
GIC_SH_MAP015_VPE31_0	32	0	rw	
GIC_SH_MAP016_VPE31_0	32	0	rw	
GIC_SH_MAP017_VPE31_0	32	0	rw	
GIC_SH_MAP018_VPE31_0	32	0	rw	
GIC_SH_MAP019_VPE31_0	32	0	rw	
GIC_SH_MAP020_VPE31_0	32	0	rw	
GIC_SH_MAP021_VPE31_0	32	0	rw	
GIC_SH_MAP022_VPE31_0	32	0	rw	
GIC_SH_MAP023_VPE31_0	32	0	rw	
GIC_SH_MAP024_VPE31_0	32	0	rw	
GIC_SH_MAP025_VPE31_0	32	0	rw	
GIC_SH_MAP026_VPE31_0	32	0	rw	
GIC_SH_MAP027_VPE31_0	32	0	rw	
GIC_SH_MAP028_VPE31_0	32	0	rw	
GIC_SH_MAP029_VPE31_0	32	0	rw	
GIC_SH_MAP030_VPE31_0	32	0	rw	
GIC_SH_MAP031_VPE31_0	32	0	rw	
GIC_SH_MAP032_VPE31_0	32	0	rw	
GIC_SH_MAP033_VPE31_0	32	0	rw	

GIC_SH_MAP034_VPE31_0	32	0	rw	
GIC_SH_MAP035_VPE31_0	32	0	rw	
GIC_SH_MAP036_VPE31_0	32	0	rw	
GIC_SH_MAP037_VPE31_0	32	0	rw	
GIC_SH_MAP038_VPE31_0	32	0	rw	
GIC_SH_MAP039_VPE31_0	32	0	rw	
GIC_SH_MAP040_VPE31_0	32	0	rw	
GIC_SH_MAP041_VPE31_0	32	0	rw	
GIC_SH_MAP042_VPE31_0	32	0	rw	
GIC_SH_MAP043_VPE31_0	32	0	rw	
GIC_SH_MAP044_VPE31_0	32	0	rw	
GIC_SH_MAP045_VPE31_0	32	0	rw	
GIC_SH_MAP046_VPE31_0	32	0	rw	
GIC_SH_MAP047_VPE31_0	32	0	rw	
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GIC_SH_MAP112_VPE31_0	32	0	rw	
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GIC_SH_MAP115_VPE31_0	32	0	rw	
GIC_SH_MAP116_VPE31_0	32	0	rw	
GIC_SH_MAP117_VPE31_0	32	0	rw	

GIC_SH_MAP118_VPE31_0	32	0	rw	
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GIC_SH_MAP201_VPE31_0	32	0	rw	

GIC_SH_MAP202_VPE31_0	32	0	rw	
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GIC_SH_MAP231_VPE31_0	32	0	rw	
GIC_SH_MAP232_VPE31_0	32	0	rw	
GIC_SH_MAP233_VPE31_0	32	0	rw	
GIC_SH_MAP234_VPE31_0	32	0	rw	
GIC_SH_MAP235_VPE31_0	32	0	rw	
GIC_SH_MAP236_VPE31_0	32	0	rw	
GIC_SH_MAP237_VPE31_0	32	0	rw	
GIC_SH_MAP238_VPE31_0	32	0	rw	
GIC_SH_MAP239_VPE31_0	32	0	rw	
GIC_SH_MAP240_VPE31_0	32	0	rw	
GIC_SH_MAP241_VPE31_0	32	0	rw	
GIC_SH_MAP242_VPE31_0	32	0	rw	
GIC_SH_MAP243_VPE31_0	32	0	rw	

GIC_SH_MAP244_VPE31_0	32	0	rw	
GIC_SH_MAP245_VPE31_0	32	0	rw	
GIC_SH_MAP246_VPE31_0	32	0	rw	
GIC_SH_MAP247_VPE31_0	32	0	rw	
GIC_SH_MAP248_VPE31_0	32	0	rw	
GIC_SH_MAP249_VPE31_0	32	0	rw	
GIC_SH_MAP250_VPE31_0	32	0	rw	
GIC_SH_MAP251_VPE31_0	32	0	rw	
GIC_SH_MAP252_VPE31_0	32	0	rw	
GIC_SH_MAP253_VPE31_0	32	0	rw	
GIC_SH_MAP254_VPE31_0	32	0	rw	
GIC_SH_MAP255_VPE31_0	32	0	rw	
GIC_VB_DINT_SEND	32	0	-w	
GIC_VPE_CTL_L	32	a	rw	
GIC_VPE_PEND_L	32	0	r-	
GIC_VPE_MASK_L	32	7f	r-	
GIC_VPE_RMASK_L	32	0	-w	
GIC_VPE_SMASK_L	32	0	-w	
GIC_VPE_WD_MAP_L	32	40000000	rw	
GIC_VPE_COMPARE_MAP_L	32	0	rw	
GIC_VPE_TIMER_MAP_L	32	80000005	rw	
GIC_VPE_FDC_MAP_L	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_L	32	80000005	rw	
GIC_VPE_SWInt0_MAP_L	32	80000000	rw	
GIC_VPE_SWInt1_MAP_L	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_L	32	0	rw	
GIC_VPE_IDENT_L	32	0	r-	
GIC_VPE_WD_CONFIG_L	32	0	rw	
GIC_VPE_WD_COUNT_L	32	0	r-	
GIC_VPE_WD_INITIAL_L	32	0	rw	
GIC_VPE_CompareLo_L	32	ffffffff	rw	
GIC_VPE_CompareHi_L	32	ffffffff	rw	
GIC_VPE_EICSS00_L	32	0	rw	
GIC_VPE_EICSS01_L	32	0	rw	
GIC_VPE_EICSS02_L	32	0	rw	
GIC_VPE_EICSS03_L	32	0	rw	
GIC_VPE_EICSS04_L	32	0	rw	
GIC_VPE_EICSS05_L	32	0	rw	
GIC_VPE_EICSS06_L	32	0	rw	
GIC_VPE_EICSS07_L	32	0	rw	
GIC_VPE_EICSS08_L	32	0	rw	
GIC_VPE_EICSS09_L	32	0	rw	

GIC_VPE_EICSS10_L	32	0	rw	
GIC_VPE_EICSS11_L	32	0	rw	
GIC_VPE_EICSS12_L	32	0	rw	
GIC_VPE_EICSS13_L	32	0	rw	
GIC_VPE_EICSS14_L	32	0	rw	
GIC_VPE_EICSS15_L	32	0	rw	
GIC_VPE_EICSS16_L	32	0	rw	
GIC_VPE_EICSS17_L	32	0	rw	
GIC_VPE_EICSS18_L	32	0	rw	
GIC_VPE_EICSS19_L	32	0	rw	
GIC_VPE_EICSS20_L	32	0	rw	
GIC_VPE_EICSS21_L	32	0	rw	
GIC_VPE_EICSS22_L	32	0	rw	
GIC_VPE_EICSS23_L	32	0	rw	
GIC_VPE_EICSS24_L	32	0	rw	
GIC_VPE_EICSS25_L	32	0	rw	
GIC_VPE_EICSS26_L	32	0	rw	
GIC_VPE_EICSS27_L	32	0	rw	
GIC_VPE_EICSS28_L	32	0	rw	
GIC_VPE_EICSS29_L	32	0	rw	
GIC_VPE_EICSS30_L	32	0	rw	
GIC_VPE_EICSS31_L	32	0	rw	
GIC_VPE_EICSS32_L	32	0	rw	
GIC_VPE_EICSS33_L	32	0	rw	
GIC_VPE_EICSS34_L	32	0	rw	
GIC_VPE_EICSS35_L	32	0	rw	
GIC_VPE_EICSS36_L	32	0	rw	
GIC_VPE_EICSS37_L	32	0	rw	
GIC_VPE_EICSS38_L	32	0	rw	
GIC_VPE_EICSS39_L	32	0	rw	
GIC_VPE_EICSS40_L	32	0	rw	
GIC_VPE_EICSS41_L	32	0	rw	
GIC_VPE_EICSS42_L	32	0	rw	
GIC_VPE_EICSS43_L	32	0	rw	
GIC_VPE_EICSS44_L	32	0	rw	
GIC_VPE_EICSS45_L	32	0	rw	
GIC_VPE_EICSS46_L	32	0	rw	
GIC_VPE_EICSS47_L	32	0	rw	
GIC_VPE_EICSS48_L	32	0	rw	
GIC_VPE_EICSS49_L	32	0	rw	
GIC_VPE_EICSS50_L	32	0	rw	
GIC_VPE_EICSS51_L	32	0	rw	

GIC_VPE_EICSS52_L	32	0	rw	
GIC_VPE_EICSS53_L	32	0	rw	
GIC_VPE_EICSS54_L	32	0	rw	
GIC_VPE_EICSS55_L	32	0	rw	
GIC_VPE_EICSS56_L	32	0	rw	
GIC_VPE_EICSS57_L	32	0	rw	
GIC_VPE_EICSS58_L	32	0	rw	
GIC_VPE_EICSS59_L	32	0	rw	
GIC_VPE_EICSS60_L	32	0	rw	
GIC_VPE_EICSS61_L	32	0	rw	
GIC_VPE_EICSS62_L	32	0	rw	
GIC_VPE_EICSS63_L	32	0	rw	
GIC_Vx_DINT_PART_L	32	1	rw	
GIC_Cx_BRK_GROUP_L	32	0	rw	
GIC_VPE_CTL_O	32	a	rw	
GIC_VPE_PEND_O	32	0	r-	
GIC_VPE_MASK_O	32	7f	r-	
GIC_VPE_RMASK_O	32	0	-w	
GIC_VPE_SMASK_O	32	0	-w	
GIC_VPE_WD_MAP_O	32	40000000	rw	
GIC_VPE_COMPARE_MAP_O	32	0	rw	
GIC_VPE_TIMER_MAP_O	32	80000005	rw	
GIC_VPE_FDC_MAP_O	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_O	32	80000005	rw	
GIC_VPE_SWInt0_MAP_O	32	80000000	rw	
GIC_VPE_SWInt1_MAP_O	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_O	32	0	rw	
GIC_VPE_IDENT_O	32	0	r-	
GIC_VPE_WD_CONFIG_O	32	0	rw	
GIC_VPE_WD_COUNT_O	32	0	r-	
GIC_VPE_WD_INITIAL_O	32	0	rw	
GIC_VPE_CompareLo_O	32	ffffffff	rw	
GIC_VPE_CompareHi_O	32	ffffffff	rw	
GIC_VPE_EICSS00_O	32	0	rw	
GIC_VPE_EICSS01_O	32	0	rw	
GIC_VPE_EICSS02_O	32	0	rw	
GIC_VPE_EICSS03_O	32	0	rw	
GIC_VPE_EICSS04_O	32	0	rw	
GIC_VPE_EICSS05_O	32	0	rw	
GIC_VPE_EICSS06_O	32	0	rw	
GIC_VPE_EICSS07_O	32	0	rw	
GIC_VPE_EICSS08_O	32	0	rw	

GIC_VPE_EICSS09_O	32	0	rw	
GIC_VPE_EICSS10_O	32	0	rw	
GIC_VPE_EICSS11_O	32	0	rw	
GIC_VPE_EICSS12_O	32	0	rw	
GIC_VPE_EICSS13_O	32	0	rw	
GIC_VPE_EICSS14_O	32	0	rw	
GIC_VPE_EICSS15_O	32	0	rw	
GIC_VPE_EICSS16_O	32	0	rw	
GIC_VPE_EICSS17_O	32	0	rw	
GIC_VPE_EICSS18_O	32	0	rw	
GIC_VPE_EICSS19_O	32	0	rw	
GIC_VPE_EICSS20_O	32	0	rw	
GIC_VPE_EICSS21_O	32	0	rw	
GIC_VPE_EICSS22_O	32	0	rw	
GIC_VPE_EICSS23_O	32	0	rw	
GIC_VPE_EICSS24_O	32	0	rw	
GIC_VPE_EICSS25_O	32	0	rw	
GIC_VPE_EICSS26_O	32	0	rw	
GIC_VPE_EICSS27_O	32	0	rw	
GIC_VPE_EICSS28_O	32	0	rw	
GIC_VPE_EICSS29_O	32	0	rw	
GIC_VPE_EICSS30_O	32	0	rw	
GIC_VPE_EICSS31_O	32	0	rw	
GIC_VPE_EICSS32_O	32	0	rw	
GIC_VPE_EICSS33_O	32	0	rw	
GIC_VPE_EICSS34_O	32	0	rw	
GIC_VPE_EICSS35_O	32	0	rw	
GIC_VPE_EICSS36_O	32	0	rw	
GIC_VPE_EICSS37_O	32	0	rw	
GIC_VPE_EICSS38_O	32	0	rw	
GIC_VPE_EICSS39_O	32	0	rw	
GIC_VPE_EICSS40_O	32	0	rw	
GIC_VPE_EICSS41_O	32	0	rw	
GIC_VPE_EICSS42_O	32	0	rw	
GIC_VPE_EICSS43_O	32	0	rw	
GIC_VPE_EICSS44_O	32	0	rw	
GIC_VPE_EICSS45_O	32	0	rw	
GIC_VPE_EICSS46_O	32	0	rw	
GIC_VPE_EICSS47_O	32	0	rw	
GIC_VPE_EICSS48_O	32	0	rw	
GIC_VPE_EICSS49_O	32	0	rw	
GIC_VPE_EICSS50_O	32	0	rw	

GIC_VPE_EICSS51_O	32	0	rw	
GIC_VPE_EICSS52_O	32	0	rw	
GIC_VPE_EICSS53_O	32	0	rw	
GIC_VPE_EICSS54_O	32	0	rw	
GIC_VPE_EICSS55_O	32	0	rw	
GIC_VPE_EICSS56_O	32	0	rw	
GIC_VPE_EICSS57_O	32	0	rw	
GIC_VPE_EICSS58_O	32	0	rw	
GIC_VPE_EICSS59_O	32	0	rw	
GIC_VPE_EICSS60_O	32	0	rw	
GIC_VPE_EICSS61_O	32	0	rw	
GIC_VPE_EICSS62_O	32	0	rw	
GIC_VPE_EICSS63_O	32	0	rw	
GIC_Vx_DINT_PART_O	32	1	rw	
GIC_Cx_BRK_GROUP_O	32	0	rw	
GIC_CounterLoUser	32	0	r-	
GIC_CounterHiUser	32	0	r-	

12.4 Level 4: TC

12.4.1 Core

Table 17.

Name	Bits	Initial value (Hex)		Description
zero	32	0	r-	constant zero
at	32	0	rw	
v0	32	0	rw	
v1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
t0	32	0	rw	
t1	32	0	rw	
t2	32	0	rw	
t3	32	0	rw	
t4	32	0	rw	
t5	32	0	rw	
t6	32	0	rw	
t7	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
s2	32	0	rw	

s3	32	0	rw	
s4	32	0	rw	
s5	32	0	rw	
s6	32	0	rw	
s7	32	0	rw	
t8	32	0	rw	
t9	32	0	rw	
k0	32	0	rw	
k1	32	0	rw	
gp	32	0	rw	
sp	32	0	rw	stack pointer
s8	32	0	rw	frame pointer
ra	32	0	rw	
pc	32	bfc00000	rw	program counter

12.4.2 DSP

Table 18.

Name	Bits	Initial value (Hex)		Description
lo	32	0	rw	
hi	32	0	rw	
lo1	32	0	rw	
hi1	32	0	rw	
lo2	32	0	rw	
hi2	32	0	rw	
lo3	32	0	rw	
hi3	32	0	rw	
dspctl	32	0	rw	DSP control

12.4.3 COP0

Table 19.

Name	Bits	Initial value (Hex)		Description
sr	32	400004	rw	CP0 register 12/0 (status)
bad	32	0	rw	CP0 register 8/0 (badvaaddr)
cause	32	0	rw	CP0 register 13/0 (cause)
index	32	0	rw	CP0 register 0/0
mvpcontrol	32	0	rw	CP0 register 0/1
mvpconf0	32	88008401	rw	CP0 register 0/2
mvpconf1	32	0	rw	CP0 register 0/3
random	32	0	rw	CP0 register 1/0
vpecontrol	32	0	rw	CP0 register 1/1

vpeconf0	32	80000003	rw	CP0 register 1/2
vpeconf1	32	0	rw	CP0 register 1/3
yqmask	32	0	rw	CP0 register 1/4
vpeschedule	32	0	rw	CP0 register 1/5
vpeschefback	32	0	rw	CP0 register 1/6
vpeopt	32	0	rw	CP0 register 1/7
entrylo0	32	0	rw	CP0 register 2/0
tcstatus	32	2000	rw	CP0 register 2/1
tcbind	32	0	rw	CP0 register 2/2
tcrestart	32	0	rw	CP0 register 2/3
tchalt	32	0	rw	CP0 register 2/4
tccontext	32	0	rw	CP0 register 2/5
tcschedule	32	0	rw	CP0 register 2/6
tcschefback	32	0	rw	CP0 register 2/7
entrylo1	32	0	rw	CP0 register 3/0
tcopt	32	0	rw	CP0 register 3/7
context	32	0	rw	CP0 register 4/0
userlocal	32	0	rw	CP0 register 4/2
pagemask	32	0	rw	CP0 register 5/0
wired	32	0	rw	CP0 register 6/0
srsconf0	32	3fffffff	rw	CP0 register 6/1
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
count	32	0	rw	CP0 register 9/0
entryhi	32	0	rw	CP0 register 10/0
compare	32	0	rw	CP0 register 11/0
status	32	400004	rw	CP0 register 12/0
intctl	32	e0000000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
epc	32	0	rw	CP0 register 14/0
prid	32	19900	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
cmgcrbase	32	1fbf800	rw	CP0 register 15/3
config	32	80048482	rw	CP0 register 16/0
config1	32	9e231186	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	20002424	rw	CP0 register 16/3
config7	32	80080100	rw	CP0 register 16/7
lladdr	32	0	rw	CP0 register 17/0
debug	32	2028000	rw	CP0 register 23/0
depc	32	0	rw	CP0 register 24/0

errctl	32	0	rw	CP0 register 26/0
itaglo	32	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	32	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
dtaghi	32	0	rw	CP0 register 29/2
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0

12.4.4 CMP_GCR

Table 20.

Name	Bits	Initial value (Hex)		Description
GCR_CONFIG	32	3	r-	
GCR_BASE	32	1fbf8000	rw	
GCR_CONTROL	32	10001	rw	
GCR_ACCESS	32	ff	rw	
GCR_REV	32	0	r-	
GCR_ERROR_MASK	32	0	rw	
GCR_ERROR_CAUSE	32	0	rw	
GCR_ERROR_ADDR	32	0	rw	
GCR_ERROR_MULT	32	0	rw	
GCR_GIC_BASE	32	0	rw	
GCR_CPC_BASE	32	0	rw	
GCR_GIC_STATUS	32	1	r-	
GCR_CACHE_REV	32	0	r-	
GCR_CPC_STATUS	32	1	r-	
GCR_IOCU1_REV	32	0	r-	
GCR_CL_RESET_RELEASE_L	32	0	-w	
GCR_CL_COHERENCE_L	32	0	rw	
GCR_CL_CONFIG_L	32	1	r-	
GCR_CL_OTHER_L	32	0	rw	
GCR_CL_RESET_BASE_L	32	bfc00000	rw	
GCR_CL_ID_L	32	0	r-	
GCR_CL_RESET_RELEASE_O	32	0	-w	
GCR_CL_COHERENCE_O	32	0	rw	
GCR_CL_CONFIG_O	32	1	r-	

GCR_CL_OTHER_O	32	0	rw	
GCR_CL_RESET_BASE_O	32	bfc00000	rw	
GCR_CL_ID_O	32	0	r-	

12.4.5 CMP_CPC

Table 21.

Name	Bits	Initial value (Hex)		Description
CPC_ACCESS	32	ff	rw	
CPC_SEQDEL	32	0	rw	
CPC_RAIL	32	0	rw	
CPC_RESETLEN	32	0	rw	
CPC_REVISION	32	0	r-	
CPC_CMD_L	32	0	rw	
CPC_STAT_CONF_L	32	380200	rw	
CPC_OTHER_L	32	0	rw	
CPC_CMD_O	32	0	rw	
CPC_STAT_CONF_O	32	380200	rw	
CPC_OTHER_O	32	0	rw	

12.4.6 CMP_GIC

Table 22.

Name	Bits	Initial value (Hex)		Description
GIC_SH_CONFIG	32	8040007	rw	
GIC_CounterLo	32	0	rw	
GIC_CounterHi	32	0	rw	
GIC_SH_REVISION	32	0	r-	
GIC_SH_POL31_0	32	0	rw	
GIC_SH_POL63_32	32	0	rw	
GIC_SH_POL95_64	32	0	rw	
GIC_SH_POL127_96	32	0	rw	
GIC_SH_POL159_128	32	0	rw	
GIC_SH_POL191_160	32	0	rw	
GIC_SH_POL223_192	32	0	rw	
GIC_SH_POL255_224	32	0	rw	
GIC_SH_TRIG31_0	32	0	rw	
GIC_SH_TRIG63_32	32	0	rw	
GIC_SH_TRIG95_64	32	0	rw	
GIC_SH_TRIG127_96	32	0	rw	
GIC_SH_TRIG159_128	32	0	rw	
GIC_SH_TRIG191_160	32	0	rw	

GIC_SH_TRIG223_192	32	0	rw	
GIC_SH_TRIG255_224	32	0	rw	
GIC_SH_DUAL31_0	32	0	rw	
GIC_SH_DUAL63_32	32	0	rw	
GIC_SH_DUAL95_64	32	0	rw	
GIC_SH_DUAL127_96	32	0	rw	
GIC_SH_DUAL159_128	32	0	rw	
GIC_SH_DUAL191_160	32	0	rw	
GIC_SH_DUAL223_192	32	0	rw	
GIC_SH_DUAL255_224	32	0	rw	
GIC_SH_WEDGE	32	0	-w	
GIC_SH_RMASK31_0	32	0	-w	
GIC_SH_RMASK63_32	32	0	-w	
GIC_SH_RMASK95_64	32	0	-w	
GIC_SH_RMASK127_96	32	0	-w	
GIC_SH_RMASK159_128	32	0	-w	
GIC_SH_RMASK191_160	32	0	-w	
GIC_SH_RMASK223_192	32	0	-w	
GIC_SH_RMASK255_224	32	0	-w	
GIC_SH_SMASK31_0	32	0	-w	
GIC_SH_SMASK63_32	32	0	-w	
GIC_SH_SMASK95_64	32	0	-w	
GIC_SH_SMASK127_96	32	0	-w	
GIC_SH_SMASK159_128	32	0	-w	
GIC_SH_SMASK191_160	32	0	-w	
GIC_SH_SMASK223_192	32	0	-w	
GIC_SH_SMASK255_224	32	0	-w	
GIC_SH_MASK31_0	32	0	r-	
GIC_SH_MASK63_32	32	0	r-	
GIC_SH_MASK95_64	32	0	r-	
GIC_SH_MASK127_96	32	0	r-	
GIC_SH_MASK159_128	32	0	r-	
GIC_SH_MASK191_160	32	0	r-	
GIC_SH_MASK223_192	32	0	r-	
GIC_SH_MASK255_224	32	0	r-	
GIC_SH_PEND31_0	32	0	r-	
GIC_SH_PEND63_32	32	0	r-	
GIC_SH_PEND95_64	32	0	r-	
GIC_SH_PEND127_96	32	0	r-	
GIC_SH_PEND159_128	32	0	r-	
GIC_SH_PEND191_160	32	0	r-	
GIC_SH_PEND223_192	32	0	r-	

GIC_SH_PEND255_224	32	0	r-	
GIC_SH_MAP000_PIN	32	80000000	rw	
GIC_SH_MAP001_PIN	32	80000000	rw	
GIC_SH_MAP002_PIN	32	80000000	rw	
GIC_SH_MAP003_PIN	32	80000000	rw	
GIC_SH_MAP004_PIN	32	80000000	rw	
GIC_SH_MAP005_PIN	32	80000000	rw	
GIC_SH_MAP006_PIN	32	80000000	rw	
GIC_SH_MAP007_PIN	32	80000000	rw	
GIC_SH_MAP008_PIN	32	80000000	rw	
GIC_SH_MAP009_PIN	32	80000000	rw	
GIC_SH_MAP010_PIN	32	80000000	rw	
GIC_SH_MAP011_PIN	32	80000000	rw	
GIC_SH_MAP012_PIN	32	80000000	rw	
GIC_SH_MAP013_PIN	32	80000000	rw	
GIC_SH_MAP014_PIN	32	80000000	rw	
GIC_SH_MAP015_PIN	32	80000000	rw	
GIC_SH_MAP016_PIN	32	80000000	rw	
GIC_SH_MAP017_PIN	32	80000000	rw	
GIC_SH_MAP018_PIN	32	80000000	rw	
GIC_SH_MAP019_PIN	32	80000000	rw	
GIC_SH_MAP020_PIN	32	80000000	rw	
GIC_SH_MAP021_PIN	32	80000000	rw	
GIC_SH_MAP022_PIN	32	80000000	rw	
GIC_SH_MAP023_PIN	32	80000000	rw	
GIC_SH_MAP024_PIN	32	80000000	rw	
GIC_SH_MAP025_PIN	32	80000000	rw	
GIC_SH_MAP026_PIN	32	80000000	rw	
GIC_SH_MAP027_PIN	32	80000000	rw	
GIC_SH_MAP028_PIN	32	80000000	rw	
GIC_SH_MAP029_PIN	32	80000000	rw	
GIC_SH_MAP030_PIN	32	80000000	rw	
GIC_SH_MAP031_PIN	32	80000000	rw	
GIC_SH_MAP032_PIN	32	80000000	rw	
GIC_SH_MAP033_PIN	32	80000000	rw	
GIC_SH_MAP034_PIN	32	80000000	rw	
GIC_SH_MAP035_PIN	32	80000000	rw	
GIC_SH_MAP036_PIN	32	80000000	rw	
GIC_SH_MAP037_PIN	32	80000000	rw	
GIC_SH_MAP038_PIN	32	80000000	rw	
GIC_SH_MAP039_PIN	32	80000000	rw	
GIC_SH_MAP040_PIN	32	80000000	rw	

GIC_SH_MAP041_PIN	32	80000000	rw	
GIC_SH_MAP042_PIN	32	80000000	rw	
GIC_SH_MAP043_PIN	32	80000000	rw	
GIC_SH_MAP044_PIN	32	80000000	rw	
GIC_SH_MAP045_PIN	32	80000000	rw	
GIC_SH_MAP046_PIN	32	80000000	rw	
GIC_SH_MAP047_PIN	32	80000000	rw	
GIC_SH_MAP048_PIN	32	80000000	rw	
GIC_SH_MAP049_PIN	32	80000000	rw	
GIC_SH_MAP050_PIN	32	80000000	rw	
GIC_SH_MAP051_PIN	32	80000000	rw	
GIC_SH_MAP052_PIN	32	80000000	rw	
GIC_SH_MAP053_PIN	32	80000000	rw	
GIC_SH_MAP054_PIN	32	80000000	rw	
GIC_SH_MAP055_PIN	32	80000000	rw	
GIC_SH_MAP056_PIN	32	80000000	rw	
GIC_SH_MAP057_PIN	32	80000000	rw	
GIC_SH_MAP058_PIN	32	80000000	rw	
GIC_SH_MAP059_PIN	32	80000000	rw	
GIC_SH_MAP060_PIN	32	80000000	rw	
GIC_SH_MAP061_PIN	32	80000000	rw	
GIC_SH_MAP062_PIN	32	80000000	rw	
GIC_SH_MAP063_PIN	32	80000000	rw	
GIC_SH_MAP064_PIN	32	80000000	rw	
GIC_SH_MAP065_PIN	32	80000000	rw	
GIC_SH_MAP066_PIN	32	80000000	rw	
GIC_SH_MAP067_PIN	32	80000000	rw	
GIC_SH_MAP068_PIN	32	80000000	rw	
GIC_SH_MAP069_PIN	32	80000000	rw	
GIC_SH_MAP070_PIN	32	80000000	rw	
GIC_SH_MAP071_PIN	32	80000000	rw	
GIC_SH_MAP072_PIN	32	80000000	rw	
GIC_SH_MAP073_PIN	32	80000000	rw	
GIC_SH_MAP074_PIN	32	80000000	rw	
GIC_SH_MAP075_PIN	32	80000000	rw	
GIC_SH_MAP076_PIN	32	80000000	rw	
GIC_SH_MAP077_PIN	32	80000000	rw	
GIC_SH_MAP078_PIN	32	80000000	rw	
GIC_SH_MAP079_PIN	32	80000000	rw	
GIC_SH_MAP080_PIN	32	80000000	rw	
GIC_SH_MAP081_PIN	32	80000000	rw	
GIC_SH_MAP082_PIN	32	80000000	rw	

GIC_SH_MAP083_PIN	32	80000000	rw	
GIC_SH_MAP084_PIN	32	80000000	rw	
GIC_SH_MAP085_PIN	32	80000000	rw	
GIC_SH_MAP086_PIN	32	80000000	rw	
GIC_SH_MAP087_PIN	32	80000000	rw	
GIC_SH_MAP088_PIN	32	80000000	rw	
GIC_SH_MAP089_PIN	32	80000000	rw	
GIC_SH_MAP090_PIN	32	80000000	rw	
GIC_SH_MAP091_PIN	32	80000000	rw	
GIC_SH_MAP092_PIN	32	80000000	rw	
GIC_SH_MAP093_PIN	32	80000000	rw	
GIC_SH_MAP094_PIN	32	80000000	rw	
GIC_SH_MAP095_PIN	32	80000000	rw	
GIC_SH_MAP096_PIN	32	80000000	rw	
GIC_SH_MAP097_PIN	32	80000000	rw	
GIC_SH_MAP098_PIN	32	80000000	rw	
GIC_SH_MAP099_PIN	32	80000000	rw	
GIC_SH_MAP100_PIN	32	80000000	rw	
GIC_SH_MAP101_PIN	32	80000000	rw	
GIC_SH_MAP102_PIN	32	80000000	rw	
GIC_SH_MAP103_PIN	32	80000000	rw	
GIC_SH_MAP104_PIN	32	80000000	rw	
GIC_SH_MAP105_PIN	32	80000000	rw	
GIC_SH_MAP106_PIN	32	80000000	rw	
GIC_SH_MAP107_PIN	32	80000000	rw	
GIC_SH_MAP108_PIN	32	80000000	rw	
GIC_SH_MAP109_PIN	32	80000000	rw	
GIC_SH_MAP110_PIN	32	80000000	rw	
GIC_SH_MAP111_PIN	32	80000000	rw	
GIC_SH_MAP112_PIN	32	80000000	rw	
GIC_SH_MAP113_PIN	32	80000000	rw	
GIC_SH_MAP114_PIN	32	80000000	rw	
GIC_SH_MAP115_PIN	32	80000000	rw	
GIC_SH_MAP116_PIN	32	80000000	rw	
GIC_SH_MAP117_PIN	32	80000000	rw	
GIC_SH_MAP118_PIN	32	80000000	rw	
GIC_SH_MAP119_PIN	32	80000000	rw	
GIC_SH_MAP120_PIN	32	80000000	rw	
GIC_SH_MAP121_PIN	32	80000000	rw	
GIC_SH_MAP122_PIN	32	80000000	rw	
GIC_SH_MAP123_PIN	32	80000000	rw	
GIC_SH_MAP124_PIN	32	80000000	rw	

GIC_SH_MAP125_PIN	32	80000000	rw	
GIC_SH_MAP126_PIN	32	80000000	rw	
GIC_SH_MAP127_PIN	32	80000000	rw	
GIC_SH_MAP128_PIN	32	80000000	rw	
GIC_SH_MAP129_PIN	32	80000000	rw	
GIC_SH_MAP130_PIN	32	80000000	rw	
GIC_SH_MAP131_PIN	32	80000000	rw	
GIC_SH_MAP132_PIN	32	80000000	rw	
GIC_SH_MAP133_PIN	32	80000000	rw	
GIC_SH_MAP134_PIN	32	80000000	rw	
GIC_SH_MAP135_PIN	32	80000000	rw	
GIC_SH_MAP136_PIN	32	80000000	rw	
GIC_SH_MAP137_PIN	32	80000000	rw	
GIC_SH_MAP138_PIN	32	80000000	rw	
GIC_SH_MAP139_PIN	32	80000000	rw	
GIC_SH_MAP140_PIN	32	80000000	rw	
GIC_SH_MAP141_PIN	32	80000000	rw	
GIC_SH_MAP142_PIN	32	80000000	rw	
GIC_SH_MAP143_PIN	32	80000000	rw	
GIC_SH_MAP144_PIN	32	80000000	rw	
GIC_SH_MAP145_PIN	32	80000000	rw	
GIC_SH_MAP146_PIN	32	80000000	rw	
GIC_SH_MAP147_PIN	32	80000000	rw	
GIC_SH_MAP148_PIN	32	80000000	rw	
GIC_SH_MAP149_PIN	32	80000000	rw	
GIC_SH_MAP150_PIN	32	80000000	rw	
GIC_SH_MAP151_PIN	32	80000000	rw	
GIC_SH_MAP152_PIN	32	80000000	rw	
GIC_SH_MAP153_PIN	32	80000000	rw	
GIC_SH_MAP154_PIN	32	80000000	rw	
GIC_SH_MAP155_PIN	32	80000000	rw	
GIC_SH_MAP156_PIN	32	80000000	rw	
GIC_SH_MAP157_PIN	32	80000000	rw	
GIC_SH_MAP158_PIN	32	80000000	rw	
GIC_SH_MAP159_PIN	32	80000000	rw	
GIC_SH_MAP160_PIN	32	80000000	rw	
GIC_SH_MAP161_PIN	32	80000000	rw	
GIC_SH_MAP162_PIN	32	80000000	rw	
GIC_SH_MAP163_PIN	32	80000000	rw	
GIC_SH_MAP164_PIN	32	80000000	rw	
GIC_SH_MAP165_PIN	32	80000000	rw	
GIC_SH_MAP166_PIN	32	80000000	rw	

GIC_SH_MAP167_PIN	32	80000000	rw	
GIC_SH_MAP168_PIN	32	80000000	rw	
GIC_SH_MAP169_PIN	32	80000000	rw	
GIC_SH_MAP170_PIN	32	80000000	rw	
GIC_SH_MAP171_PIN	32	80000000	rw	
GIC_SH_MAP172_PIN	32	80000000	rw	
GIC_SH_MAP173_PIN	32	80000000	rw	
GIC_SH_MAP174_PIN	32	80000000	rw	
GIC_SH_MAP175_PIN	32	80000000	rw	
GIC_SH_MAP176_PIN	32	80000000	rw	
GIC_SH_MAP177_PIN	32	80000000	rw	
GIC_SH_MAP178_PIN	32	80000000	rw	
GIC_SH_MAP179_PIN	32	80000000	rw	
GIC_SH_MAP180_PIN	32	80000000	rw	
GIC_SH_MAP181_PIN	32	80000000	rw	
GIC_SH_MAP182_PIN	32	80000000	rw	
GIC_SH_MAP183_PIN	32	80000000	rw	
GIC_SH_MAP184_PIN	32	80000000	rw	
GIC_SH_MAP185_PIN	32	80000000	rw	
GIC_SH_MAP186_PIN	32	80000000	rw	
GIC_SH_MAP187_PIN	32	80000000	rw	
GIC_SH_MAP188_PIN	32	80000000	rw	
GIC_SH_MAP189_PIN	32	80000000	rw	
GIC_SH_MAP190_PIN	32	80000000	rw	
GIC_SH_MAP191_PIN	32	80000000	rw	
GIC_SH_MAP192_PIN	32	80000000	rw	
GIC_SH_MAP193_PIN	32	80000000	rw	
GIC_SH_MAP194_PIN	32	80000000	rw	
GIC_SH_MAP195_PIN	32	80000000	rw	
GIC_SH_MAP196_PIN	32	80000000	rw	
GIC_SH_MAP197_PIN	32	80000000	rw	
GIC_SH_MAP198_PIN	32	80000000	rw	
GIC_SH_MAP199_PIN	32	80000000	rw	
GIC_SH_MAP200_PIN	32	80000000	rw	
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GIC_SH_MAP202_PIN	32	80000000	rw	
GIC_SH_MAP203_PIN	32	80000000	rw	
GIC_SH_MAP204_PIN	32	80000000	rw	
GIC_SH_MAP205_PIN	32	80000000	rw	
GIC_SH_MAP206_PIN	32	80000000	rw	
GIC_SH_MAP207_PIN	32	80000000	rw	
GIC_SH_MAP208_PIN	32	80000000	rw	

GIC_SH_MAP209_PIN	32	80000000	rw	
GIC_SH_MAP210_PIN	32	80000000	rw	
GIC_SH_MAP211_PIN	32	80000000	rw	
GIC_SH_MAP212_PIN	32	80000000	rw	
GIC_SH_MAP213_PIN	32	80000000	rw	
GIC_SH_MAP214_PIN	32	80000000	rw	
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GIC_SH_MAP216_PIN	32	80000000	rw	
GIC_SH_MAP217_PIN	32	80000000	rw	
GIC_SH_MAP218_PIN	32	80000000	rw	
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GIC_SH_MAP220_PIN	32	80000000	rw	
GIC_SH_MAP221_PIN	32	80000000	rw	
GIC_SH_MAP222_PIN	32	80000000	rw	
GIC_SH_MAP223_PIN	32	80000000	rw	
GIC_SH_MAP224_PIN	32	80000000	rw	
GIC_SH_MAP225_PIN	32	80000000	rw	
GIC_SH_MAP226_PIN	32	80000000	rw	
GIC_SH_MAP227_PIN	32	80000000	rw	
GIC_SH_MAP228_PIN	32	80000000	rw	
GIC_SH_MAP229_PIN	32	80000000	rw	
GIC_SH_MAP230_PIN	32	80000000	rw	
GIC_SH_MAP231_PIN	32	80000000	rw	
GIC_SH_MAP232_PIN	32	80000000	rw	
GIC_SH_MAP233_PIN	32	80000000	rw	
GIC_SH_MAP234_PIN	32	80000000	rw	
GIC_SH_MAP235_PIN	32	80000000	rw	
GIC_SH_MAP236_PIN	32	80000000	rw	
GIC_SH_MAP237_PIN	32	80000000	rw	
GIC_SH_MAP238_PIN	32	80000000	rw	
GIC_SH_MAP239_PIN	32	80000000	rw	
GIC_SH_MAP240_PIN	32	80000000	rw	
GIC_SH_MAP241_PIN	32	80000000	rw	
GIC_SH_MAP242_PIN	32	80000000	rw	
GIC_SH_MAP243_PIN	32	80000000	rw	
GIC_SH_MAP244_PIN	32	80000000	rw	
GIC_SH_MAP245_PIN	32	80000000	rw	
GIC_SH_MAP246_PIN	32	80000000	rw	
GIC_SH_MAP247_PIN	32	80000000	rw	
GIC_SH_MAP248_PIN	32	80000000	rw	
GIC_SH_MAP249_PIN	32	80000000	rw	
GIC_SH_MAP250_PIN	32	80000000	rw	

GIC_SH_MAP251_PIN	32	80000000	rw	
GIC_SH_MAP252_PIN	32	80000000	rw	
GIC_SH_MAP253_PIN	32	80000000	rw	
GIC_SH_MAP254_PIN	32	80000000	rw	
GIC_SH_MAP255_PIN	32	80000000	rw	
GIC_SH_MAP000_VPE31_0	32	0	rw	
GIC_SH_MAP001_VPE31_0	32	0	rw	
GIC_SH_MAP002_VPE31_0	32	0	rw	
GIC_SH_MAP003_VPE31_0	32	0	rw	
GIC_SH_MAP004_VPE31_0	32	0	rw	
GIC_SH_MAP005_VPE31_0	32	0	rw	
GIC_SH_MAP006_VPE31_0	32	0	rw	
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GIC_SH_MAP008_VPE31_0	32	0	rw	
GIC_SH_MAP009_VPE31_0	32	0	rw	
GIC_SH_MAP010_VPE31_0	32	0	rw	
GIC_SH_MAP011_VPE31_0	32	0	rw	
GIC_SH_MAP012_VPE31_0	32	0	rw	
GIC_SH_MAP013_VPE31_0	32	0	rw	
GIC_SH_MAP014_VPE31_0	32	0	rw	
GIC_SH_MAP015_VPE31_0	32	0	rw	
GIC_SH_MAP016_VPE31_0	32	0	rw	
GIC_SH_MAP017_VPE31_0	32	0	rw	
GIC_SH_MAP018_VPE31_0	32	0	rw	
GIC_SH_MAP019_VPE31_0	32	0	rw	
GIC_SH_MAP020_VPE31_0	32	0	rw	
GIC_SH_MAP021_VPE31_0	32	0	rw	
GIC_SH_MAP022_VPE31_0	32	0	rw	
GIC_SH_MAP023_VPE31_0	32	0	rw	
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GIC_SH_MAP025_VPE31_0	32	0	rw	
GIC_SH_MAP026_VPE31_0	32	0	rw	
GIC_SH_MAP027_VPE31_0	32	0	rw	
GIC_SH_MAP028_VPE31_0	32	0	rw	
GIC_SH_MAP029_VPE31_0	32	0	rw	
GIC_SH_MAP030_VPE31_0	32	0	rw	
GIC_SH_MAP031_VPE31_0	32	0	rw	
GIC_SH_MAP032_VPE31_0	32	0	rw	
GIC_SH_MAP033_VPE31_0	32	0	rw	
GIC_SH_MAP034_VPE31_0	32	0	rw	
GIC_SH_MAP035_VPE31_0	32	0	rw	
GIC_SH_MAP036_VPE31_0	32	0	rw	

GIC_SH_MAP037_VPE31_0	32	0	rw	
GIC_SH_MAP038_VPE31_0	32	0	rw	
GIC_SH_MAP039_VPE31_0	32	0	rw	
GIC_SH_MAP040_VPE31_0	32	0	rw	
GIC_SH_MAP041_VPE31_0	32	0	rw	
GIC_SH_MAP042_VPE31_0	32	0	rw	
GIC_SH_MAP043_VPE31_0	32	0	rw	
GIC_SH_MAP044_VPE31_0	32	0	rw	
GIC_SH_MAP045_VPE31_0	32	0	rw	
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GIC_SH_MAP048_VPE31_0	32	0	rw	
GIC_SH_MAP049_VPE31_0	32	0	rw	
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GIC_SH_MAP053_VPE31_0	32	0	rw	
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GIC_SH_MAP071_VPE31_0	32	0	rw	
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GIC_SH_MAP073_VPE31_0	32	0	rw	
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GIC_SH_MAP078_VPE31_0	32	0	rw	

GIC_SH_MAP079_VPE31_0	32	0	rw	
GIC_SH_MAP080_VPE31_0	32	0	rw	
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GIC_SH_MAP086_VPE31_0	32	0	rw	
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GIC_SH_MAP088_VPE31_0	32	0	rw	
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GIC_SH_MAP103_VPE31_0	32	0	rw	
GIC_SH_MAP104_VPE31_0	32	0	rw	
GIC_SH_MAP105_VPE31_0	32	0	rw	
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GIC_SH_MAP107_VPE31_0	32	0	rw	
GIC_SH_MAP108_VPE31_0	32	0	rw	
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GIC_SH_MAP111_VPE31_0	32	0	rw	
GIC_SH_MAP112_VPE31_0	32	0	rw	
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GIC_SH_MAP114_VPE31_0	32	0	rw	
GIC_SH_MAP115_VPE31_0	32	0	rw	
GIC_SH_MAP116_VPE31_0	32	0	rw	
GIC_SH_MAP117_VPE31_0	32	0	rw	
GIC_SH_MAP118_VPE31_0	32	0	rw	
GIC_SH_MAP119_VPE31_0	32	0	rw	
GIC_SH_MAP120_VPE31_0	32	0	rw	

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GIC_SH_MAP122_VPE31_0	32	0	rw	
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GIC_SH_MAP165_VPE31_0	32	0	rw	
GIC_SH_MAP166_VPE31_0	32	0	rw	
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GIC_SH_MAP171_VPE31_0	32	0	rw	
GIC_SH_MAP172_VPE31_0	32	0	rw	
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GIC_SH_MAP174_VPE31_0	32	0	rw	
GIC_SH_MAP175_VPE31_0	32	0	rw	
GIC_SH_MAP176_VPE31_0	32	0	rw	
GIC_SH_MAP177_VPE31_0	32	0	rw	
GIC_SH_MAP178_VPE31_0	32	0	rw	
GIC_SH_MAP179_VPE31_0	32	0	rw	
GIC_SH_MAP180_VPE31_0	32	0	rw	
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GIC_SH_MAP182_VPE31_0	32	0	rw	
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GIC_SH_MAP185_VPE31_0	32	0	rw	
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GIC_SH_MAP187_VPE31_0	32	0	rw	
GIC_SH_MAP188_VPE31_0	32	0	rw	
GIC_SH_MAP189_VPE31_0	32	0	rw	
GIC_SH_MAP190_VPE31_0	32	0	rw	
GIC_SH_MAP191_VPE31_0	32	0	rw	
GIC_SH_MAP192_VPE31_0	32	0	rw	
GIC_SH_MAP193_VPE31_0	32	0	rw	
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GIC_SH_MAP212_VPE31_0	32	0	rw	
GIC_SH_MAP213_VPE31_0	32	0	rw	
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GIC_SH_MAP219_VPE31_0	32	0	rw	
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GIC_SH_MAP221_VPE31_0	32	0	rw	
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GIC_SH_MAP223_VPE31_0	32	0	rw	
GIC_SH_MAP224_VPE31_0	32	0	rw	
GIC_SH_MAP225_VPE31_0	32	0	rw	
GIC_SH_MAP226_VPE31_0	32	0	rw	
GIC_SH_MAP227_VPE31_0	32	0	rw	
GIC_SH_MAP228_VPE31_0	32	0	rw	
GIC_SH_MAP229_VPE31_0	32	0	rw	
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GIC_SH_MAP231_VPE31_0	32	0	rw	
GIC_SH_MAP232_VPE31_0	32	0	rw	
GIC_SH_MAP233_VPE31_0	32	0	rw	
GIC_SH_MAP234_VPE31_0	32	0	rw	
GIC_SH_MAP235_VPE31_0	32	0	rw	
GIC_SH_MAP236_VPE31_0	32	0	rw	
GIC_SH_MAP237_VPE31_0	32	0	rw	
GIC_SH_MAP238_VPE31_0	32	0	rw	
GIC_SH_MAP239_VPE31_0	32	0	rw	
GIC_SH_MAP240_VPE31_0	32	0	rw	
GIC_SH_MAP241_VPE31_0	32	0	rw	
GIC_SH_MAP242_VPE31_0	32	0	rw	
GIC_SH_MAP243_VPE31_0	32	0	rw	
GIC_SH_MAP244_VPE31_0	32	0	rw	
GIC_SH_MAP245_VPE31_0	32	0	rw	
GIC_SH_MAP246_VPE31_0	32	0	rw	

GIC_SH_MAP247_VPE31_0	32	0	rw	
GIC_SH_MAP248_VPE31_0	32	0	rw	
GIC_SH_MAP249_VPE31_0	32	0	rw	
GIC_SH_MAP250_VPE31_0	32	0	rw	
GIC_SH_MAP251_VPE31_0	32	0	rw	
GIC_SH_MAP252_VPE31_0	32	0	rw	
GIC_SH_MAP253_VPE31_0	32	0	rw	
GIC_SH_MAP254_VPE31_0	32	0	rw	
GIC_SH_MAP255_VPE31_0	32	0	rw	
GIC_VB_DINT_SEND	32	0	-w	
GIC_VPE_CTL_L	32	a	rw	
GIC_VPE_PEND_L	32	0	r-	
GIC_VPE_MASK_L	32	7f	r-	
GIC_VPE_RMASK_L	32	0	-w	
GIC_VPE_SMASK_L	32	0	-w	
GIC_VPE_WD_MAP_L	32	40000000	rw	
GIC_VPE_COMPARE_MAP_L	32	0	rw	
GIC_VPE_TIMER_MAP_L	32	80000005	rw	
GIC_VPE_FDC_MAP_L	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_L	32	80000005	rw	
GIC_VPE_SWInt0_MAP_L	32	80000000	rw	
GIC_VPE_SWInt1_MAP_L	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_L	32	0	rw	
GIC_VPE_IDENT_L	32	0	r-	
GIC_VPE_WD_CONFIG_L	32	0	rw	
GIC_VPE_WD_COUNT_L	32	0	r-	
GIC_VPE_WD_INITIAL_L	32	0	rw	
GIC_VPE_CompareLo_L	32	ffffffff	rw	
GIC_VPE_CompareHi_L	32	ffffffff	rw	
GIC_VPE_EICSS00_L	32	0	rw	
GIC_VPE_EICSS01_L	32	0	rw	
GIC_VPE_EICSS02_L	32	0	rw	
GIC_VPE_EICSS03_L	32	0	rw	
GIC_VPE_EICSS04_L	32	0	rw	
GIC_VPE_EICSS05_L	32	0	rw	
GIC_VPE_EICSS06_L	32	0	rw	
GIC_VPE_EICSS07_L	32	0	rw	
GIC_VPE_EICSS08_L	32	0	rw	
GIC_VPE_EICSS09_L	32	0	rw	
GIC_VPE_EICSS10_L	32	0	rw	
GIC_VPE_EICSS11_L	32	0	rw	
GIC_VPE_EICSS12_L	32	0	rw	

GIC_VPE_EICSS13_L	32	0	rw	
GIC_VPE_EICSS14_L	32	0	rw	
GIC_VPE_EICSS15_L	32	0	rw	
GIC_VPE_EICSS16_L	32	0	rw	
GIC_VPE_EICSS17_L	32	0	rw	
GIC_VPE_EICSS18_L	32	0	rw	
GIC_VPE_EICSS19_L	32	0	rw	
GIC_VPE_EICSS20_L	32	0	rw	
GIC_VPE_EICSS21_L	32	0	rw	
GIC_VPE_EICSS22_L	32	0	rw	
GIC_VPE_EICSS23_L	32	0	rw	
GIC_VPE_EICSS24_L	32	0	rw	
GIC_VPE_EICSS25_L	32	0	rw	
GIC_VPE_EICSS26_L	32	0	rw	
GIC_VPE_EICSS27_L	32	0	rw	
GIC_VPE_EICSS28_L	32	0	rw	
GIC_VPE_EICSS29_L	32	0	rw	
GIC_VPE_EICSS30_L	32	0	rw	
GIC_VPE_EICSS31_L	32	0	rw	
GIC_VPE_EICSS32_L	32	0	rw	
GIC_VPE_EICSS33_L	32	0	rw	
GIC_VPE_EICSS34_L	32	0	rw	
GIC_VPE_EICSS35_L	32	0	rw	
GIC_VPE_EICSS36_L	32	0	rw	
GIC_VPE_EICSS37_L	32	0	rw	
GIC_VPE_EICSS38_L	32	0	rw	
GIC_VPE_EICSS39_L	32	0	rw	
GIC_VPE_EICSS40_L	32	0	rw	
GIC_VPE_EICSS41_L	32	0	rw	
GIC_VPE_EICSS42_L	32	0	rw	
GIC_VPE_EICSS43_L	32	0	rw	
GIC_VPE_EICSS44_L	32	0	rw	
GIC_VPE_EICSS45_L	32	0	rw	
GIC_VPE_EICSS46_L	32	0	rw	
GIC_VPE_EICSS47_L	32	0	rw	
GIC_VPE_EICSS48_L	32	0	rw	
GIC_VPE_EICSS49_L	32	0	rw	
GIC_VPE_EICSS50_L	32	0	rw	
GIC_VPE_EICSS51_L	32	0	rw	
GIC_VPE_EICSS52_L	32	0	rw	
GIC_VPE_EICSS53_L	32	0	rw	
GIC_VPE_EICSS54_L	32	0	rw	

GIC_VPE_EICSS55_L	32	0	rw	
GIC_VPE_EICSS56_L	32	0	rw	
GIC_VPE_EICSS57_L	32	0	rw	
GIC_VPE_EICSS58_L	32	0	rw	
GIC_VPE_EICSS59_L	32	0	rw	
GIC_VPE_EICSS60_L	32	0	rw	
GIC_VPE_EICSS61_L	32	0	rw	
GIC_VPE_EICSS62_L	32	0	rw	
GIC_VPE_EICSS63_L	32	0	rw	
GIC_Vx_DINT_PART_L	32	1	rw	
GIC_Cx_BRK_GROUP_L	32	0	rw	
GIC_VPE_CTL_O	32	a	rw	
GIC_VPE_PEND_O	32	0	r-	
GIC_VPE_MASK_O	32	7f	r-	
GIC_VPE_RMASK_O	32	0	-w	
GIC_VPE_SMASK_O	32	0	-w	
GIC_VPE_WD_MAP_O	32	40000000	rw	
GIC_VPE_COMPARE_MAP_O	32	0	rw	
GIC_VPE_TIMER_MAP_O	32	80000005	rw	
GIC_VPE_FDC_MAP_O	32	8000003e	rw	
GIC_VPE_PERFCTR_MAP_O	32	80000005	rw	
GIC_VPE_SWInt0_MAP_O	32	80000000	rw	
GIC_VPE_SWInt1_MAP_O	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS_O	32	0	rw	
GIC_VPE_IDENT_O	32	0	r-	
GIC_VPE_WD_CONFIG_O	32	0	rw	
GIC_VPE_WD_COUNT_O	32	0	r-	
GIC_VPE_WD_INITIAL_O	32	0	rw	
GIC_VPE_CompareLo_O	32	ffffffff	rw	
GIC_VPE_CompareHi_O	32	ffffffff	rw	
GIC_VPE_EICSS00_O	32	0	rw	
GIC_VPE_EICSS01_O	32	0	rw	
GIC_VPE_EICSS02_O	32	0	rw	
GIC_VPE_EICSS03_O	32	0	rw	
GIC_VPE_EICSS04_O	32	0	rw	
GIC_VPE_EICSS05_O	32	0	rw	
GIC_VPE_EICSS06_O	32	0	rw	
GIC_VPE_EICSS07_O	32	0	rw	
GIC_VPE_EICSS08_O	32	0	rw	
GIC_VPE_EICSS09_O	32	0	rw	
GIC_VPE_EICSS10_O	32	0	rw	
GIC_VPE_EICSS11_O	32	0	rw	

GIC_VPE_EICSS12_O	32	0	rw	
GIC_VPE_EICSS13_O	32	0	rw	
GIC_VPE_EICSS14_O	32	0	rw	
GIC_VPE_EICSS15_O	32	0	rw	
GIC_VPE_EICSS16_O	32	0	rw	
GIC_VPE_EICSS17_O	32	0	rw	
GIC_VPE_EICSS18_O	32	0	rw	
GIC_VPE_EICSS19_O	32	0	rw	
GIC_VPE_EICSS20_O	32	0	rw	
GIC_VPE_EICSS21_O	32	0	rw	
GIC_VPE_EICSS22_O	32	0	rw	
GIC_VPE_EICSS23_O	32	0	rw	
GIC_VPE_EICSS24_O	32	0	rw	
GIC_VPE_EICSS25_O	32	0	rw	
GIC_VPE_EICSS26_O	32	0	rw	
GIC_VPE_EICSS27_O	32	0	rw	
GIC_VPE_EICSS28_O	32	0	rw	
GIC_VPE_EICSS29_O	32	0	rw	
GIC_VPE_EICSS30_O	32	0	rw	
GIC_VPE_EICSS31_O	32	0	rw	
GIC_VPE_EICSS32_O	32	0	rw	
GIC_VPE_EICSS33_O	32	0	rw	
GIC_VPE_EICSS34_O	32	0	rw	
GIC_VPE_EICSS35_O	32	0	rw	
GIC_VPE_EICSS36_O	32	0	rw	
GIC_VPE_EICSS37_O	32	0	rw	
GIC_VPE_EICSS38_O	32	0	rw	
GIC_VPE_EICSS39_O	32	0	rw	
GIC_VPE_EICSS40_O	32	0	rw	
GIC_VPE_EICSS41_O	32	0	rw	
GIC_VPE_EICSS42_O	32	0	rw	
GIC_VPE_EICSS43_O	32	0	rw	
GIC_VPE_EICSS44_O	32	0	rw	
GIC_VPE_EICSS45_O	32	0	rw	
GIC_VPE_EICSS46_O	32	0	rw	
GIC_VPE_EICSS47_O	32	0	rw	
GIC_VPE_EICSS48_O	32	0	rw	
GIC_VPE_EICSS49_O	32	0	rw	
GIC_VPE_EICSS50_O	32	0	rw	
GIC_VPE_EICSS51_O	32	0	rw	
GIC_VPE_EICSS52_O	32	0	rw	
GIC_VPE_EICSS53_O	32	0	rw	

GIC_VPE_EICSS54_O	32	0	rw	
GIC_VPE_EICSS55_O	32	0	rw	
GIC_VPE_EICSS56_O	32	0	rw	
GIC_VPE_EICSS57_O	32	0	rw	
GIC_VPE_EICSS58_O	32	0	rw	
GIC_VPE_EICSS59_O	32	0	rw	
GIC_VPE_EICSS60_O	32	0	rw	
GIC_VPE_EICSS61_O	32	0	rw	
GIC_VPE_EICSS62_O	32	0	rw	
GIC_VPE_EICSS63_O	32	0	rw	
GIC_Vx_DINT_PART_O	32	1	rw	
GIC_Cx_BRK_GROUP_O	32	0	rw	
GIC_CounterLoUser	32	0	r-	
GIC_CounterHiUser	32	0	r-	

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Table 23.

Name	Bits	Initial value (Hex)		Description
stop	32	0	rw	write with non-zero to stop processor

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