OVP Guide to Using Processor Models

Model Specific Information for variant MIPS32_34Kn

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1.0 Overview

This document provides the details of an OVP Fast Processor Model variant.
OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms. The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance.
Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.
The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.
There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS32 Configurable Processor Model

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

MIPS32 Instruction set implemented
MMU Type: Fixed Mapping
L1 I and D cache model in either full or tag-only mode implemented (disabled by default)
Vectored interrupts implemented
MIPS16e ASE implemented
MT ASE implemented
DSP ASE implemented

2.0 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
    mips.ovpworld.org/processor/mips32/1.0

2.2 GDB Path

The default GDB for this model is found at:
    $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/mips-sde-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
    mips.ovpworld.org/semihosting/mips32SDE/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 Processor ELF Code

The ELF code supported by this model is: 0x8

3.0 Other Variants in this Model

Table 1.

Variant
ISA
M14K
M14KcTLB
M14KcFMM
4KEc
4KEm
4KEp
M4K
4Kc
4Km
4Kp
24Kc
24Kf
24KEc
24KEf
34Kc
34Kf
34Kn
74Kc
74Kf
1004Kc
1004Kf
1074Kc
1074Kf
microAptivC
microAptivP
interAptiv
proAptiv

4.0 Bus Ports

Table 2.

Type	Name	Bits
master (initiator)	INSTRUCTION	32
master (initiator)	DATA	32

5.0 Net Ports

Table 3.

Name	Type	Description

yq	input	Yield qualifier
reset	input	Core reset
dint	input	Debug external interrupt
hwint0_VPE0	input	External interrupt
hwint1_VPE0	input	External interrupt
hwint2_VPE0	input	External interrupt
hwint3_VPE0	input	External interrupt
hwint4_VPE0	input	External interrupt
hwint5_VPE0	input	External interrupt
nmi_VPE0	input	Non-maskable external interrupt
hwint0	input	External interrupt for compatibility
hwint0_VPE1	input	External interrupt
hwint1_VPE1	input	External interrupt
hwint2_VPE1	input	External interrupt
hwint3_VPE1	input	External interrupt
hwint4_VPE1	input	External interrupt
hwint5_VPE1	input	External interrupt
nmi_VPE1	input	Non-maskable external interrupt

6.0 FIFO Ports

No FIFO Ports in this model.

7.0 Parameters

Table 4.

Name	Type	Description
cacheenable	Enumeration	Select cache model mode default=0 tag=1 full=2
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)
mipsHexFile	String	Load a MIPS hex file (test-mode)
MIPS_TRACE	Boolean	Enable MIPS-format trace output
MIPS16eASE	Boolean	Enables the MIPS16e ASE
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions

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fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
config3ULRI	Boolean	Override the ULRI field in Config3 register
config3ISAOnExc	Boolean	Override the ISAOnExc field in Config3 register
config3MCU	Boolean	Override the MCU field in Config3 register
config3CDMM	Boolean	Override the CDMM field in Config3 register
config3SC	Boolean	Override the SC field in Config3 register
config4AE	Boolean	Override the AE field in Config4 register
config5EVA	Boolean	Override the EVA field in Config5 register
isISA	Uns32	Set to 1 to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Uns32	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
ITCNumEntries	Uns32	Specify number of ITC cells present (MT cores only)
ITCNumFIFO	Uns32	Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mvpconf0vpe	Uns32	Override the PVPE field in MVPConf0 register
mvpconf0tc	Uns32	Override the PTC field in MVPConf0 register
mvpconf0pcp	Uns32	Override the PCP field in MVPConf0 register
mvpconf0tcp	Uns32	Override the TCP field in MVPConf0 register
configK0	Uns32	Override the power on value for the K0 field of the Config register (set Kseg0 cacheability)
configKU	Uns32	Override the power on value for the KU field of the Config register (set Useg cacheability)
configK23	Uns32	Override the power on value for the K23 field of the Config register (set Kseg23 cacheability)
configMT	Uns32	Override the MT field in Config register
configISP	Uns32	Override the ISP field in Config register (instruction scratchpad RAM present)
configDSP	Uns32	Override the DSP field in Config register (data scratchpad RAM present)
configSB	Uns32	Override the SB field in Config register (simple bus transfers only)

config1MMUSizeM1	Uns32	Override the MMUSizeM1 field in Config1 register (number of MMU entries-1)
config1IS	Uns32	Override the IS field in Config1 register (Icache sets per way)
config1IL	Uns32	Override the IL field in Config1 register (Icache line size)
config1IA	Uns32	Override the IA field in Config1 register (Icache associativity)
config1DS	Uns32	Override the DS field in Config1 register (Dcache sets per way)
config1DL	Uns32	Override the DL field in Config1 register (Dcache line size)
config1DA	Uns32	Override the DA field in Config1 register (Dcache associativity)
config1EP	Uns32	Override the EP field in Config1 register (EJTag present)
config1WR	Uns32	Override the WR field in Config1 register (Watchpoint registers present)
config3ISA	Uns32	Override the ISA field in Config3 register
config3MMAR	Uns32	Override the MMAR field in Config3 register
config3IPLW	Uns32	Override the IPLW field in Config3 register
config3RXI	Uns32	Override the RXI field in Config3 register
config3DSPP	Uns32	Override the DSPP field in Config3 register
config3DSP2P	Uns32	Override the DSP2P field in Config3 register
config3CTXTC	Uns32	Override the CTXTC field in Config3 register
config3ITL	Uns32	Override the ITL field in Config3 register
config4IE	Uns32	Override the IE field in Config4 register
config4VTLBSizeExt	Uns32	Override the VTLBSizeExt field in Config4 register
config4MMUExtDef	Uns32	Override the MMUExtDef field in Config4 register
config4MMUConfig	Uns32	Override the MMUConfig field (bits 12:0) in Config4 register (interpretation depends on MMUExtDef value)
config6FTLBEn	Uns32	Override the power on value for the FTLBEn field of the Config6 register
config7AR	Uns32	Override the AR field in Config7 register (Alias removed Data cache)
config7IAR	Uns32	Override the IAR field in Config7 register (Alias removed Instruction cache)
config7WII	Uns32	Override the WII field in Config7 register (wait IE/IXMT ignore)
config7HCI	Uns32	Override the HCI field in Config7 register (Hardware Cache Initialization)
config7DCIDX_MODE	Uns32	

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srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
pridRevision	Uns32	Override the Revision field in PRId register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
BEVBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
firstBEVBaseMaskBit	Uns32	Specify LSB position of BEVBaseMask (defines minimum BEV overlay size). Only used when SegCtl enabled
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location Only used when non-CMP and SegCtl enabled
BEVBaseMask	Uns32	Specify the BEVBaseMask value used for bits [27:firstBEVBaseMaskBit]. Only used when non-CMP and SegCtl enabled
LegacyUseBEVBase	Boolean	Set to one to use BEVBase[29:12] as the corresponding BEV address bits even when Config5.K==0. Only used when non-CMP and SegCtl enabled
BEVBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl enabled
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present
TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override the PCORES field in GCR_CONFIG register (number of cores-1)
GCR_BASE	Uns32	CMP system only: override the GCR_BASE field in GCR_BASE register (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override the MINOR_REV field in GCR_REV register
GCR_MAJOR_REV	Uns32	CMP system only: override the MAJOR_REV field in GCR_REV register
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override the MINOR_REV field in GCR_CACHE_REV register
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override the MAJOR_REV field in GCR_CACHE_REV register
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override the MINOR_REV field in GCR_IOCU1_REV register
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override the MAJOR_REV field in GCR_IOCU1_REV register

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GIC_NUMINTERRUPTS	Uns32	CMP system only: override the NUMINTERRUPTS field in GIC_SH_CONFIG register
GIC_COUNTBITS	Uns32	CMP system only: override the COUNTBITS field in GIC_SH_CONFIG register
GIC_MINOR_REV	Uns32	CMP system only: override the MINOR_REV field in GIC_SH_REVISION register
GIC_MAJOR_REV	Uns32	CMP system only: override the MAJOR_REV field in GIC_SH_REVISION register
CPC_MICROSTEP	Uns32	CMP system only: override the MICROSTEP field in CPC_SEQDEL register
CPC_RAILDELAY	Uns32	CMP system only: override the RAILDELAY field in CPC_RAIL register
CPC_RESETLEN	Uns32	CMP system only: override the RESETLEN field in CPC_RESETLEN register
CPC_MINOR_REV	Uns32	CMP system only: override the MINOR_REV field in CPC_REVISION register
CPC_MAJOR_REV	Uns32	CMP system only: override the MAJOR_REV field in CPC_REVISION register
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0. Only used when SegCtl enabled
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1. Only used when SegCtl enabled
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2. Only used when SegCtl enabled
GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3. Only used when SegCtl enabled
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION

8.0 Execution Modes

Table 5.

Name	Code
KERNEL	0

DEBUG	1
SUPERVISOR	2
USER	3

9.0 Exceptions

Table 6.

Name	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Bp	9
RI	10
CpU	11
Ov	12
Tr	13
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
Prot	29
CacheErr	30

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10.0 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1: CPU

This level in the model hierarchy has no commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has 2 children:

PE0 and PE1

10.2 Level 2: VPE

This level in the model hierarchy has no commands.

This level in the model hierarchy has one register group:

Table 7.

Group name	Registers
COP0	42

This level in the model hierarchy has one child:

C0

10.3 Level 3: TC

This level in the model hierarchy has 10 commands.

This level in the model hierarchy has 3 register groups:

Table 8.

Group name	Registers
Core	33
DSP	9
COP0	55

This level in the model hierarchy has no children.

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11.0 Model Commands

11.1 Level 1: CPU

No commands.

11.2 Level 2: VPE

No commands.

11.3 Level 3: TC

Table 9.

Name	Arguments
mipsCOP0	{register} {select}
mipsCacheDisable	
mipsCacheEnable	-tag|-full
mipsCacheRatio	-icache|-dcache
mipsCacheReport	
mipsCacheReset	
mipsCacheTrace	-on|-off [-nocached|-nouncached] [-noicache|-nodcache] [-noartifact|-notrue]
mipsDebugFlags	{value}
mipsReadRegister	{resource} {offset}
mipsWriteRegister	{resource} {offset} {value}

12.0 Registers

12.1 Level 1: CPU

No registers.

12.2 Level 2: VPE

12.2.1 COP0

Table 10.

Name	Bits	Initial value (Hex)		Description
bad	32	0	rw	CP0 register 8/0
cause	32	0	rw	CP0 register 13/0
mvpcontrol	32	0	rw	CP0 register 0/1
mvpconf0	32	c8008401	rw	CP0 register 0/2
mvpconf1	32	0	rw	CP0 register 0/3
vpecontrol	32	0	rw	CP0 register 1/1
vpeconf0	32	80000003	rw	CP0 register 1/2

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vpeconf1	32	0	rw	CP0 register 1/3
yqmask	32	0	rw	CP0 register 1/4
vpeschedule	32	0	rw	CP0 register 1/5
vpeschefback	32	0	rw	CP0 register 1/6
vpeopt	32	0	rw	CP0 register 1/7
srsconf0	32	3fffffff	rw	CP0 register 6/1
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
count	32	0	rw	CP0 register 9/0
compare	32	0	rw	CP0 register 11/0
intctl	32	e0000000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
epc	32	0	rw	CP0 register 14/0
prid	32	19500	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
config	32	a4048582	rw	CP0 register 16/0
config1	32	80231186	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	2424	rw	CP0 register 16/3
config7	32	80080000	rw	CP0 register 16/7
depc	32	0	rw	CP0 register 24/0
errctl	32	0	rw	CP0 register 26/0
itaglo	32	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	32	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
dtaghi	32	0	rw	CP0 register 29/2
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0

12.3 Level 3: TC

12.3.1 Core

Table 11.

Name	Bits	Initial value (Hex)		Description

zero	32	0	r-	constant zero
at	32	0	rw	
v0	32	0	rw	
v1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
t0	32	0	rw	
t1	32	0	rw	
t2	32	0	rw	
t3	32	0	rw	
t4	32	0	rw	
t5	32	0	rw	
t6	32	0	rw	
t7	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
s2	32	0	rw	
s3	32	0	rw	
s4	32	0	rw	
s5	32	0	rw	
s6	32	0	rw	
s7	32	0	rw	
t8	32	0	rw	
t9	32	0	rw	
k0	32	0	rw	
k1	32	0	rw	
gp	32	0	rw	
sp	32	0	rw	stack pointer
s8	32	0	rw	frame pointer
ra	32	0	rw	
pc	32	bfc00000	rw	program counter

12.3.2 DSP

Table 12.

Name	**Bits**	**Initial value (Hex)**		**Description**
lo	32	0	rw	
hi	32	0	rw	
lo1	32	0	rw	
hi1	32	0	rw	

lo2	32	0	rw	
hi2	32	0	rw	
lo3	32	0	rw	
hi3	32	0	rw	
dspctl	32	0	rw	DSP control

12.3.3 COP0

Table 13.

Name	Bits	Initial value (Hex)		Description
sr	32	400004	rw	CP0 register 12/0
bad	32	0	rw	CP0 register 8/0
cause	32	0	rw	CP0 register 13/0
mvpcontrol	32	0	rw	CP0 register 0/1
mvpconf0	32	c8008401	rw	CP0 register 0/2
mvpconf1	32	0	rw	CP0 register 0/3
vpecontrol	32	0	rw	CP0 register 1/1
vpeconf0	32	80000003	rw	CP0 register 1/2
vpeconf1	32	0	rw	CP0 register 1/3
yqmask	32	0	rw	CP0 register 1/4
vpeschedule	32	0	rw	CP0 register 1/5
vpeschefback	32	0	rw	CP0 register 1/6
vpeopt	32	0	rw	CP0 register 1/7
tcstatus	32	2000	rw	CP0 register 2/1
tcbind	32	0	rw	CP0 register 2/2
tcrestart	32	0	rw	CP0 register 2/3
tchalt	32	0	rw	CP0 register 2/4
tccontext	32	0	rw	CP0 register 2/5
tcschedule	32	0	rw	CP0 register 2/6
tcschefback	32	0	rw	CP0 register 2/7
tcopt	32	0	rw	CP0 register 3/7
userlocal	32	0	rw	CP0 register 4/2
srsconf0	32	3fffffff	rw	CP0 register 6/1
hwrena	32	0	rw	CP0 register 7/0
badvaddr	32	0	rw	CP0 register 8/0
count	32	0	rw	CP0 register 9/0
compare	32	0	rw	CP0 register 11/0
status	32	400004	rw	CP0 register 12/0
intctl	32	e0000000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
epc	32	0	rw	CP0 register 14/0

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prid	32	19500	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1
config	32	a4048582	rw	CP0 register 16/0
config1	32	80231186	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	2424	rw	CP0 register 16/3
config7	32	80080000	rw	CP0 register 16/7
lladdr	32	0	rw	CP0 register 17/0
debug	32	2028000	rw	CP0 register 23/0
depc	32	0	rw	CP0 register 24/0
errctl	32	0	rw	CP0 register 26/0
itaglo	32	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	32	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
dtaghi	32	0	rw	CP0 register 29/2
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0

#

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