OVP Guide to Using Processor Models

Model Specific Information for variant MIPS32_P5600

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Table of Contents

1 Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance.

Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners.

There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS32 Configurable Processor Model

If you need other variants, these models can be obtained from www.OVPworld.org/MIPSuser.

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPSuser.

Cache model does not implement coherency

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

MIPS32 Instruction set implemented

MMU Type: Standard TLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Segmentation control implemented

Enhanced virtual address (EVA) supported

Vectored interrupts implemented

2 Configuration

2.1 Location

The model source and object file is found in the VLNV tree at:
imgtec.ovpworld.org/processor/mips32/1.0

2.2 GDB Path

The default GDB for this model is found at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/CrossCompiler/mips-mti-elf/2016.05-03/bin/mips-mti-elf-gdb

2.3 Semi-Host Library

The default semi-host library file is found in the VLNV tree at :
mips.ovpworld.org/semihosting/mips32Newlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF Code

The ELF code supported by this model is: 0x8

3 Other Variants in this Model

Table 1. All variants in this model

Variant
M5100
.M5100Guest
M5150
.M5150Guest
M6200
M6250
MIPS32R6
.MIPS32R6Guest
P5600
.P5600Guest

4 Bus Ports

Table 2. Bus Ports

Type	Name	min	max
master (initiator)	INSTRUCTION	37	59
master (initiator)	DATA	37	59

5 Net Ports

Table 3. Net Ports

Name	Type	Description
reset	input	CMP reset
dint	input	Debug external interrupt
int0	input	GIC external interrupt
int1	input	GIC external interrupt
int2	input	GIC external interrupt
int3	input	GIC external interrupt
int4	input	GIC external interrupt
int5	input	GIC external interrupt
int6	input	GIC external interrupt
int7	input	GIC external interrupt
int8	input	GIC external interrupt
int9	input	GIC external interrupt
int10	input	GIC external interrupt
int11	input	GIC external interrupt
int12	input	GIC external interrupt
int13	input	GIC external interrupt
int14	input	GIC external interrupt
int15	input	GIC external interrupt
int16	input	GIC external interrupt
int17	input	GIC external interrupt
int18	input	GIC external interrupt
int19	input	GIC external interrupt
int20	input	GIC external interrupt
int21	input	GIC external interrupt
int22	input	GIC external interrupt
int23	input	GIC external interrupt
int24	input	GIC external interrupt
int25	input	GIC external interrupt
int26	input	GIC external interrupt
int27	input	GIC external interrupt
int28	input	GIC external interrupt
int29	input	GIC external interrupt
int30	input	GIC external interrupt
int31	input	GIC external interrupt
int32	input	GIC external interrupt
int33	input	GIC external interrupt
int34	input	GIC external interrupt
int35	input	GIC external interrupt
int36	input	GIC external interrupt
int37	input	GIC external interrupt

int38	input	GIC external interrupt
int39	input	GIC external interrupt
ej_disable_probe_debug	input	GIC ej_disable_probe_debug
ejtagbrk_override	input	GIC ejtagbrk_override
ej_dint_in	input	GIC ej_dint_in
GCR_CUSTOM_BASE	output	Provides the least significant 32-bits of the value written to the GCR_CUSTOM_BASE register. Second half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
GCR_CUSTOM_BASE_UPPER	output	Provides the most significant 32-bits of value written to the the GCR_CUSTOM_BASE register. First half of GCR_CUSTOM_BASE_HI and GCR_CUSTOM_BASE output.
reset_CPU0	input	Core reset
hwint0_CPU0	input	External interrupt
hwint1_CPU0	input	External interrupt
hwint2_CPU0	input	External interrupt
hwint3_CPU0	input	External interrupt
hwint4_CPU0	input	External interrupt
hwint5_CPU0	input	External interrupt
nmi_CPU0	input	Non-maskable external interrupt
EICPresent_CPU0	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU0	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU0	input	External interrupt controller EICSS
EIC_VectorNum_CPU0	input	External interrupt controller vector number
EIC_VectorOffset_CPU0	input	External interrupt controller vector offset
EIC_GID_CPU0	input	External interrupt controller guest ID
intISS_CPU0	output	True when interrupt request is serviced
causeTI_CPU0	output	True when timer interrupt expires
causeIP0_CPU0	output	Raised for software interrupt request IP0
causeIP1_CPU0	output	Raised for software interrupt request IP1
si_sleep_CPU0	output	True when the VPE is in WAIT state
hwint0	input	External interrupt for compatibility
Guest.EIC_RIPL_CPU0	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU0	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU0	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU0	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU0	input	Guest External interrupt controller guest ID
Guest.intISS_CPU0	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU0	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU0	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU0	output	Raised for Guest software interrupt request IP1

reset_CPU1	input	Core reset
hwint0_CPU1	input	External interrupt
hwint1_CPU1	input	External interrupt
hwint2_CPU1	input	External interrupt
hwint3_CPU1	input	External interrupt
hwint4_CPU1	input	External interrupt
hwint5_CPU1	input	External interrupt
nmi_CPU1	input	Non-maskable external interrupt
EICPresent_CPU1	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU1	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU1	input	External interrupt controller EICSS
EIC_VectorNum_CPU1	input	External interrupt controller vector number
EIC_VectorOffset_CPU1	input	External interrupt controller vector offset
EIC_GID_CPU1	input	External interrupt controller guest ID
intISS_CPU1	output	True when interrupt request is serviced
causeTI_CPU1	output	True when timer interrupt expires
causeIP0_CPU1	output	Raised for software interrupt request IP0
causeIP1_CPU1	output	Raised for software interrupt request IP1
si_sleep_CPU1	output	True when the VPE is in WAIT state
Guest.EIC_RIPL_CPU1	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU1	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU1	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU1	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU1	input	Guest External interrupt controller guest ID
Guest.intISS_CPU1	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU1	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU1	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU1	output	Raised for Guest software interrupt request IP1
reset_CPU2	input	Core reset
hwint0_CPU2	input	External interrupt
hwint1_CPU2	input	External interrupt
hwint2_CPU2	input	External interrupt
hwint3_CPU2	input	External interrupt
hwint4_CPU2	input	External interrupt
hwint5_CPU2	input	External interrupt
nmi_CPU2	input	Non-maskable external interrupt
EICPresent_CPU2	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU2	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU2	input	External interrupt controller EICSS
EIC_VectorNum_CPU2	input	External interrupt controller vector number

EIC_VectorOffset_CPU2	input	External interrupt controller vector offset
EIC_GID_CPU2	input	External interrupt controller guest ID
intISS_CPU2	output	True when interrupt request is serviced
causeTI_CPU2	output	True when timer interrupt expires
causeIP0_CPU2	output	Raised for software interrupt request IP0
causeIP1_CPU2	output	Raised for software interrupt request IP1
si_sleep_CPU2	output	True when the VPE is in WAIT state
Guest.EIC_RIPL_CPU2	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU2	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU2	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU2	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU2	input	Guest External interrupt controller guest ID
Guest.intISS_CPU2	output	True when Guest interrupt request is serviced
Guest.causeTI_CPU2	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU2	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU2	output	Raised for Guest software interrupt request IP1
reset_CPU3	input	Core reset
hwint0_CPU3	input	External interrupt
hwint1_CPU3	input	External interrupt
hwint2_CPU3	input	External interrupt
hwint3_CPU3	input	External interrupt
hwint4_CPU3	input	External interrupt
hwint5_CPU3	input	External interrupt
nmi_CPU3	input	Non-maskable external interrupt
EICPresent_CPU3	input	Input signal SI_EICPresent per VPE
EIC_RIPL_CPU3	input	External interrupt controller RIPL (alias of hwint0 - 5 or 7)
EIC_EICSS_CPU3	input	External interrupt controller EICSS
EIC_VectorNum_CPU3	input	External interrupt controller vector number
EIC_VectorOffset_CPU3	input	External interrupt controller vector offset
EIC_GID_CPU3	input	External interrupt controller guest ID
intISS_CPU3	output	True when interrupt request is serviced
causeTI_CPU3	output	True when timer interrupt expires
causeIP0_CPU3	output	Raised for software interrupt request IP0
causeIP1_CPU3	output	Raised for software interrupt request IP1
si_sleep_CPU3	output	True when the VPE is in WAIT state
Guest.EIC_RIPL_CPU3	input	Guest External interrupt controller RIPL
Guest.EIC_EICSS_CPU3	input	Guest External interrupt controller EICSS
Guest.EIC_VectorNum_CPU3	input	Guest External interrupt controller vector number
Guest.EIC_VectorOffset_CPU3	input	Guest External interrupt controller vector offset
Guest.EIC_GID_CPU3	input	Guest External interrupt controller guest ID
Guest.intISS_CPU3	output	True when Guest interrupt request is serviced

Guest.causeTI_CPU3	output	True when Guest timer interrupt expires
Guest.causeIP0_CPU3	output	Raised for Guest software interrupt request IP0
Guest.causeIP1_CPU3	output	Raised for Guest software interrupt request IP1

6 FIFO Ports

No FIFO Ports in this model.

7 Parameters

Table 4. Parameters that can be set in the model, type: CMP

Name	Type	Description
cacheenable	Enumeration	Select cache model mode default=0 tag=1 full=2
cachedebug	Uns32	Cache debug flags
cacheextbiuinfo	Pointer	Pointer to platform-provided BIU cache info structure
mipsHexFile	String	Load a MIPS hex file (test-mode)
IMPERAS_MIPS_AVP_OPCODES	Boolean	Enable MIPS-specific magic Pass/ Fail opcodes (specific for AVP test termination)
cacheIndexBypassTLB	Boolean	When set, cache index ops do not generate TLB exceptions
MIPS_TRACE	Boolean	Enable MIPS-format trace output
supervisorMode	Boolean	Override whether processor implements supervisor mode
busErrors	Boolean	Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions
fixedMMU	Boolean	Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)
fixedDbgRegSize	Boolean	Enable applications to debug on P5600 with GDB version 2015.06-05 and prior
removeDSP	Boolean	Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)
removeCMP	Boolean	Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)
removeFP	Boolean	Override the FP-Present configuration when true (sets Config1.FP to 0)
removeFTLB	Boolean	Override the FTLBEn configuration when true (disable FTLB)

isISA	Boolean	Enable to specify ISA model (reset address from ELF, all coprocessors enabled)
hiddenTLBentries	Boolean	Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance
MTFPU	Uns32	Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)
supportDenormals	Boolean	Enable to specify that the FPU supports denormal operands and results
VPE0MaxTC	Uns32	Specifies the maximum TCs initially on VPE0
mpuRegions	Uns32	Number of regions for memory protection unit
mpuType	Uns32	Type of MPU implementation
mpuEnable	Boolean	Enable MPU2 segment control at reset
mpuSegment0	Uns32	Attributes for segment 0 in MPU2 SegmentControl_0 register
mpuSegment1	Uns32	Attributes for segment 1 in MPU2 SegmentControl_0 register
mpuSegment2	Uns32	Attributes for segment 2 in MPU2 SegmentControl_0 register
mpuSegment3	Uns32	Attributes for segment 3 in MPU2 SegmentControl_0 register
mpuSegment4	Uns32	Attributes for segment 4 in MPU2 SegmentControl_1 register
mpuSegment5	Uns32	Attributes for segment 5 in MPU2 SegmentControl_1 register
mpuSegment6	Uns32	Attributes for segment 6 in MPU2 SegmentControl_1 register
mpuSegment7	Uns32	Attributes for segment 7 in MPU2 SegmentControl_1 register
mpuSegment8	Uns32	Attributes for segment 8 in MPU2 SegmentControl_2 register
mpuSegment9	Uns32	Attributes for segment 9 in MPU2 SegmentControl_2 register
mpuSegment10	Uns32	Attributes for segment 10 in MPU2 SegmentControl_2 register
mpuSegment11	Uns32	Attributes for segment 11 in MPU2 SegmentControl_2 register
mpuSegment12	Uns32	Attributes for segment 12 in MPU2 SegmentControl_3 register
mpuSegment13	Uns32	Attributes for segment 13 in MPU2 SegmentControl_3 register

mpuSegment14	Uns32	Attributes for segment 14 in MPU2 SegmentControl_3 register
mpuSegment15	Uns32	Attributes for segment 15 in MPU2 SegmentControl_3 register
mvpconf0vpe	Uns32	Override MVPConf0.PVPE
mvpconf0tc	Uns32	Override MVPConf0.PTC
mvpconf0pcp	Boolean	Override MVPConf0.PCP
mvpconf0tcp	Boolean	Override MVPConf0.TCP
hasFDC	Uns32	Specify the size of Fast Debug Channel register block
licenseWarningDays	Uns32	Specify the number of days before a license expires to start issuing a warning. 0 disables warnings.
MIPS_UHI	Boolean	Enable MIPS-Unified Hosting interface
mipsUhiArgs	String	Specifies UHI arguments string seperated by spaces
mipsUhiJail	String	Specifies UHI jailroot
MIPS_DV_MODE	Boolean	Enable Design Verification mode
MIPS_MAGIC_OPCODES	Boolean	Enable MIPS-specific magic Pass/Fail opcodes
enableTrickbox	Boolean	Enable trickbox addresses (specific for AVP)
fpuexcdisable	Boolean	Disable FPU exceptions
TRU_PRESENT	Boolean	Disable or Enable based on TRU presence to control certain fields (e.x.perfCtl.PCTD
ucLLwordsLocked	Uns32	Numbers of words (4 byte) an uncached LL is locking. Maximum: 4K
cop2Bits	Uns32	Specifies width in bits of COP2 registers (32 or 64)
cop2FileName	String	Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions
udiConfig	Int32	Specifies UDI configuration attribute
udiFileName	String	Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions
vectoredinterrupt	Boolean	Enables vectored interrupts (sets Config3 VInt)
externalinterrupt	Boolean	Enables the use of an external interrupt controller (sets Config3 VEIC)
rootFixedMMU	Boolean	Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2)

rootMMUSizeM1	Uns32	Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1)
srsctlHSS	Uns32	Override the HSS field in SRSCtl register (number of shadow register sets)
firPS	Uns32	Override the PS field in FIR register
firHas2008	Uns32	Override the Has2008 field in FIR register
simulateLite	Uns32	Run Simulation with no overhead. By default runs with disabled Forbidden slot for R6 cores when set to 1.
pridCompanyOptions	Uns32	Override the Company Options field in PRId register
pridRevision	Uns32	Override the Revision field in PRId register
globalClusterNum	Uns32	Override the ClusterNum field in GlobalNumber register
intctlIPTI	Uns32	Override the IPTI field in IntCtl register
intctlIPFDC	Uns32	Override the IPFDC field in IntCtl register
intctlIPPCI	Uns32	Override the IPPCI field in IntCtl register
numWatch	Uns32	Specify number of WatchLo/WatchHi register pairs
xconfigSpecified	Boolean	True if the configuration comes from a valid xconfig file
cdmmSize	Uns32	Override the cdmmsize reset value
configAR	Uns32	Enables R6 support
configBM	Uns32	Override the BM field in Config register (burst mode)
configDSP	Boolean	Override Config.DSP (data scratchpad RAM present)
configISP	Boolean	Override Config.ISP (instruction scratchpad RAM present)
configK0	Uns32	Override power on value of Config.K0 (set Kseg0 cacheability)
configKU	Uns32	Override power on value of Config.KU (set Useg cacheability)
configK23	Uns32	Override power on value of Config.K23 (set Kseg23 cacheability)
configMDU	Boolean	Override Config.MDU (iterative multiply/divide unit)
configMM	Boolean	Override Config.MM (merging mode for write)
configMT	Uns32	Override Config.MT

configSB	Boolean	Override Config.SB (simple bus transfers only)
configBCP	Boolean	Override Config.BCP (Buffer Cache Present)
MIPS16eASE	Boolean	Override Config1.CA (enables the MIPS16e ASE)
config1DA	Uns32	Override Config1.DA (Dcache associativity)
config1DL	Uns32	Override Config1.DL (Dcache line size)
config1DS	Uns32	Override Config1.DS (Dcache sets per way)
config1EP	Boolean	Override Config1.EP (EJTag present)
config1IA	Uns32	Override Config1.IA (Icache associativity)
config1IL	Uns32	Override Config1.IL (Icache line size)
config1IS	Uns32	Override Config1.IS (Icache sets per way)
config1MMUSizeM1	Uns32	Override Config1.MMUSizeM1 (number of MMU entries-1)
config1WR	Boolean	Override Config1.WR (watchpoint registers present)
config1PC	Boolean	Override Config1.PC (Performance Counters present)
config1C2	Boolean	Override Config1.C2 (Coprocessor 2 present)
config2SU	Uns32	Override the SU field in Config2 register
config2SS	Uns32	Override the SS field in Config2 register
config2SL	Uns32	Override the SL field in Config2 register
config2SA	Uns32	Override the SA field in Config2 register
config3BI	Boolean	Override Config3.BI
config3BP	Boolean	Override Config3.BP
config3CDMM	Boolean	Override Config3.CDMM
config3CTXTC	Boolean	Override Config3.CTXTC
config3DSPP	Boolean	Override Config3.DSPP
config3DSP2P	Boolean	Override Config3.DSP2P
config3IPLW	Uns32	Override Config3.IPLW
config3ISA	Uns32	Override Config3.ISA
config3ISAOnExc	Boolean	Override Config3.ISAOnExc
config3ITL	Boolean	Override Config3.ITL
config3LPA	Boolean	Override Config3.LPA

config3MCU	Boolean	Override Config3.MCU
config3MMAR	Uns32	Override Config3.MMAR
config3RXI	Boolean	Override Config3.RXI
config3SC	Boolean	Override Config3.SC
config3ULRI	Boolean	Override Config3.ULRI
config3VZ	Boolean	Override Config3.VZ
config3MSAP	Boolean	Override Config3.MSAP
config3CMGCR	Boolean	Override the CMGCR field in Config3 register
config3SP	Boolean	Override the SP field in Config3 register
config3TL	Uns32	Override the TL field in Config3 register
config3PW	Boolean	Override the PW field in Config3 register
config4AE	Boolean	Override Config4.AE
config4IE	Uns32	Override Config4.IE
config4MMUConfig	Uns32	Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)
config4MMUExtDef	Uns32	Override Config4.MMUExtDef
config4VTLBSizeExt	Uns32	Override Config4.VTLBSizeExt
config5EVA	Boolean	Override Config5.EVA
config5LLB	Boolean	Override Config5.LLB (LLAddr supports LLbit)
config5MRP	Boolean	Override Config5.MRP (MaaR Present)
config5NFExists	Boolean	Override Config5.NFExists
mips32Macro	Boolean	Enables the MIPS32 SAVE and RESTORE macro instructions. Ignored if Config5.CA2 is not set)
config5MSAEn	Boolean	Override Config5.MSAEn
config5MVH	Boolean	Override Config5.MVH (enable MTHC0 and MFHC0 instructions)
config5DEC	Boolean	Override Config5.DEC (to test Dual Endian Capability)
config5GI	Uns32	Override Config5.GI (enable GINV)
config5CRCP	Boolean	Override Config5.CRCP (CRCP Present)
config6FTLBEn	Boolean	Override power on value of Config6.FTLBEn
config7AR	Boolean	Override Config7.AR (Alias removed Data cache)
config7DCIDX_MODE	Uns32	Override Config7.DCIDX_MODE

config7HCI	Boolean	Override Config7.HCI (Hardware Cache Initialization)
config7IAR	Boolean	Override Config7.IAR (Alias removed Instruction cache)
config7WII	Boolean	Override Config7.WII (wait IE/IXMT ignore)
config7ES	Uns32	Override the ES field in Config7 register (Externalize sync)
statusFR	Boolean	Override power on value in Status.FR (Floating point register mode)
fcsrABS2008	Boolean	Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)
fcsrNAN2008	Boolean	Override FCSR.NAN2008 (QNaN/ SNaN encodings match IEEE 754-2008 recommendation)
numMaarRegs	Uns32	Override number of MAAR registers (must be even)
wiredLimit	Uns32	Override Limit field of the Wired register
cdmmBaseCI	Boolean	Override CDMMBase.CI
ExceptionBase	Uns32	Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors)
UseExceptionBase	Boolean	Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits
firstBEVExceptionBaseMaskBit	Uns32	Specify LSB position of GCR_Cx_RESET_EXT_BASE.BEVExceptionBaseMas field. Only used when SegCtl present
EVAReset	Boolean	Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present
ExceptionBaseMask	Uns32	Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present
ExceptionBasePA	Uns32	Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present
l1BufferCache	Boolean	L1 Buffer Cache
GCU_EX	Boolean	CMP system only: GCR custom block present
GIC_EX	Boolean	CMP system only: GIC unit present
CPC_EX	Boolean	CMP system only: CPC unit present

TIMER_ROUTABLE	Boolean	CMP system only: cpu timer interrupt routable within cluster
SWINT_ROUTABLE	Boolean	CMP system only: software interrupt routable within cluster
GCR_PCORES	Uns32	CMP system only: override GCR_CONFIG.PCORES (number of cores-1)
GCR_BASE	Uns32	CMP system only: override GCR_BASE.GCR_BASE (default GCR register address)
GCR_MINOR_REV	Uns32	CMP system only: override GCR_REV.MINOR_REV
GCR_MAJOR_REV	Uns32	CMP system only: override GCR_REV.MAJOR_REV
GCR_CACHE_MINOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MINOR_REV
GCR_CACHE_MAJOR_REV	Uns32	CMP system only: override GCR_CACHE_REV.MAJOR_REV
GCR_L2_ASSOC	Uns32	CMP system only: override GCR_L2_CONFIG.ASSOC
GCR_L2_SET_SIZE	Uns32	CMP system only: override GCR_L2_CONFIG.SET_SIZE
GCR_SYS_CONFIG2_MAX_VP_WIDTH	Uns32	CMP system only: override GCR_SYS_CONFIG2.MAX_VP_WIDTH
GCR_IOCU1_MINOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MINOR_REV
GCR_IOCU1_MAJOR_REV	Uns32	CMP system only: override GCR_IOCU1_REV.MAJOR_REV
GIC_NUMINTERRUPTS	Uns32	CMP system only: override GIC_SH_CONFIG.NUMINTERRUPTS
GIC_COUNTBITS	Uns32	CMP system only: override GIC_SH_CONFIG.COUNTBITS
GIC_MINOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MINOR_REV
GIC_MAJOR_REV	Uns32	CMP system only: override GIC_SH_REVISION.MAJOR_REV
GIC_NUM_TEAMS	Uns32	CMP system only: override GIC_SH_DBG_CONFIG.NUM_TEAMS
GIC_TRIG_RESET	Uns32	CMP system only: Zero value of GIC_SH_TRIG_[31_0, 63_32]
GIC_PVPES	Uns32	CMP system only: override GIC_SH_CONFIG.PVPE
CPC_MICROSTEP	Uns32	CMP system only: override CPC_SEQDEL.MICROSTEP
CPC_RAILDELAY	Uns32	CMP system only: override CPC_RAIL.RAILDELAY

CPC_RESETLEN	Uns32	CMP system only: override CPC_RESETLEN.RESETLEN
CPC_MINOR_REV	Uns32	CMP system only: override CPC_REVISION.MINOR_REV
CPC_MAJOR_REV	Uns32	CMP system only: override CPC_REVISION.MAJOR_REV
GIC_SH_GID_CONFIG31_0	Uns32	CMP system only: override GIC_SH_GID_CONFIG[31_0]
GIC_SH_GID_CONFIG63_32	Uns32	CMP system only: override GIC_SH_GID_CONFIG[63_32]
GIC_SH_GID_CONFIG95_64	Uns32	CMP system only: override GIC_SH_GID_CONFIG[95_64]
GIC_SH_GID_CONFIG127_96	Uns32	CMP system only: override GIC_SH_GID_CONFIG[127_96]
GIC_SH_GID_CONFIG159_128	Uns32	CMP system only: override GIC_SH_GID_CONFIG[159_128]
GIC_SH_GID_CONFIG191_160	Uns32	CMP system only: override GIC_SH_GID_CONFIG[191_160]
GIC_SH_GID_CONFIG223_192	Uns32	CMP system only: override GIC_SH_GID_CONFIG[223_192]
GIC_SH_GID_CONFIG255_224	Uns32	CMP system only: override GIC_SH_GID_CONFIG[255_224]
GCR_C0_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 0
GCR_C1_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 1
GCR_C2_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 2
GCR_C3_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 3
GCR_C4_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 4
GCR_C5_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 5
GCR_C6_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 6
GCR_C7_RESET_BASE	Uns32	CMP system only: GCR_CL_RESET_BASE for core 7
GCR_C0_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 0
GCR_C1_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 1
GCR_C2_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 2

GCR_C3_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 3
GCR_C4_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 4
GCR_C5_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 5
GCR_C6_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 6
GCR_C7_RESET_EXT_BASE	Uns32	CMP system only: GCR_CL_RESET_EXT_BASE for core 7
CPC_C0_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 0
CPC_C1_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 1
CPC_C2_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 2
CPC_C3_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 3
CPC_C4_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 4
CPC_C5_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 5
CPC_C6_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 6
CPC_C7_VP_EN	Uns32	CMP system only: CPC_VP_EN for core 7
EIC_OPTION	Uns32	Override the external interrupt controller EIC_OPTION
guestCtl0RI	Uns32	Override the RI field in GuestCtl0 register
guestCtl0MC	Uns32	Override the MC field in GuestCtl0 register
guestCtl0CP0	Uns32	Override the CP0 field in GuestCtl0 register
guestCtl0AT	Uns32	Override the AT field in GuestCtl0 register
guestCtl0GT	Uns32	Override the GT field in GuestCtl0 register
guestCtl0CG	Uns32	Override the CG field in GuestCtl0 register
guestCtl0CF	Uns32	Override the CF field in GuestCtl0 register

guestCtl0G1	Uns32	Override the G1 field in GuestCtl0 register
guestCtl0RAD	Uns32	Override the RAD field in GuestCtl0 register
guestCtl0DRG	Uns32	Override the DRG field in GuestCtl0 register
hasImpl17	Boolean	Enable read/write of Impl17 bit in Status register
hasImpl16	Boolean	Enable read/write of Impl16 bit in Status register
guestintctlIPTI	Uns32	Override the Guest IPTI field in IntCtl register
guestintctlIPFDC	Uns32	Override the Guest IPFDC field in IntCtl register
guestintctlIPPCI	Uns32	Override the Guest IPPCI field in IntCtl register
ISPRAM_SIZE	Uns32	Encoded size of the ISPRAM region (log2(<ISPRAM size in bytes>) - 11)
ISPRAM_BASE	Uns64	Starting physical address of the ISPRAM region
ISPRAM_ENABLE	Boolean	Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)
ISPRAM_FILE	String	Load a MIPS hex file into the ISPRAM region prior to reset
DSPRAM_SIZE	Uns32	Encoded size of the DSPRAM region (log2(<DSPRAM size in bytes>) - 11)
DSPRAM_BASE	Uns64	Starting physical address of the DSPRAM region
DSPRAM_ENABLE	Boolean	Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset)
DSPRAM_PRESENT	Boolean	DSPRAM is present with SAAR
misalignedDataException	Enumeration	Select misaligned data access exception signaling: never, checkCCA or always never=0 checkCCA=1 always=2
commitTlbwErr	Boolean	Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only

8 Execution Modes

Table 5. CPU modes implemented in the model, type: CMP

Name	Code
KERNEL	0
DEBUG	1

SUPERVISOR	2
USER	3
GUEST_KERNEL	4
GUEST_SUPERVISOR	5
GUEST_USER	6

9 Exceptions

Table 6. Exceptions handled by the model, type: CMP

Name	Code
Int	0
Mod	1
TLBL	2
TLBS	3
AdEL	4
AdES	5
IBE	6
DBE	7
Sys	8
Bp	9
RI	10
CpU	11
Ov	12
Tr	13
MSAFPE	14
FPE	15
Impl1	16
Impl2	17
C2E	18
TLBRI	19
TLBXI	20
MSADis	21
MDMX	22
WATCH	23
MCheck	24
Thread	25
DSPDis	26
GE	27
Prot	29
CacheErr	30

10 Hierarchy of the model

A CPU core may allow the user to configure it to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy.

Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

10.1 Level 1: CMP

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has 4 children:

CPU0, CPU1, CPU2 and CPU3

10.2 Level 2: CPU

This level in the model hierarchy has 20 commands.

This level in the model hierarchy has 10 register groups:

Table 7. Register groups

Group name	Registers
Core	33
FPU	34
DSP	9
Shadow	32
COP0	154
MSA	40
CMP_GCR	38
CMP_CPC	11
CMP_GIC	746
Integration_support	1

This level in the model hierarchy has no children.

11 Model Commands

11.1 Level 1: CMP

11.1.1 isync

specify instruction address range for synchronous execution

Table 8. isync command arguments

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

11.1.2 itrace

enable or disable instruction tracing

Table 9. itrace command arguments

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

11.2 Level 2: CPU

11.2.1 isync

specify instruction address range for synchronous execution

Table 10. isync command arguments

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

11.2.2 itrace

enable or disable instruction tracing

Table 11. itrace command arguments

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction

-registers	Boolean	show registers after each trace

11.2.3 mipsCOP0
query a COP0 register value using <register> <select>

Table 12. mipsCOP0 command arguments

Argument	Type	Description
-register	Int32	specify the COP0 register resource
-select	Int32	specify the COP0 register select

11.2.4 mipsCacheDisable

11.2.4.1 Argument description
Disables tag or full cache model

11.2.5 mipsCacheEnable
enable tag or full cache model

Table 13. mipsCacheEnable command arguments

Argument	Type	Description
-debug	Int32	set cache model debug flags
-full	Boolean	enable full cache model
-tag	Boolean	enable cache tag line only model

11.2.6 mipsCacheRatio
Report current hit ratio for selected cache

Table 14. mipsCacheRatio command arguments

Argument	Type	Description
-dcache	Boolean	report hit ratio for dcache
-icache	Boolean	report hit ratio for icache

11.2.7 mipsCacheReport

11.2.7.1 Argument description
Report current cache statistics

11.2.8 mipsCacheReset

11.2.8.1 Argument description
reset the cache model

11.2.9 mipsCacheTrace
Control the tracing of cache accesses

Table 15. mipsCacheTrace command arguments

Argument	Type	Description
-noartifact	Boolean	
-nocached	Boolean	
-nodcache	Boolean	

-noicache	Boolean	
-notrue	Boolean	
-nounchched	Boolean	
-off	Boolean	turn off the cache tracing
-on	Boolean	turn on the cache tracing

11.2.10 mipsDebugFlags
Set the mips model debug value

Table 16. mipsDebugFlags command arguments

Argument	Type	Description
-value	Int32	specify mips model debug flags

11.2.11 mipsReadRegister
Read processor register using <resource> <offset>

Table 17. mipsReadRegister command arguments

Argument	Type	Description
-offset	Int32	the register offset
-resource	Int32	the register resource

11.2.12 mipsReadTLBEntry
read a TLB entry specified by the index

Table 18. mipsReadTLBEntry command arguments

Argument	Type	Description
-index	Uns64	select the TLB entry

11.2.13 mipsTLBDump
11.2.13.1 Argument description
Dumps the current contents of the TLB

11.2.14 mipsTLBDumpGuest
11.2.14.1 Argument description
Dumps the current contents of the Guest TLB

11.2.15 mipsTLBDumpRoot
11.2.15.1 Argument description
Dumps the current contents of the Root TLB

11.2.16 mipsTLBGetPhys
Reports the entry(s) in the TLB that match the given virtual address and ASID

Table 19. mipsTLBGetPhys command arguments

Argument	Type	Description
-asid	Uns64	ASID
-va	Uns64	virtual address

11.2.17 mipsTraceGuest
control tracing of guest

Table 20. mipsTraceGuest command arguments

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

11.2.18 mipsTraceRoot
control tracing on root processor

Table 21. mipsTraceRoot command arguments

Argument	Type	Description
-off	Boolean	stop tracing
-on	Boolean	start tracing

11.2.19 mipsWriteRegister
Write processor register using <resource> <offset> <value>

Table 22. mipsWriteRegister command arguments

Argument	Type	Description
-offset	Int32	the register offset
-resource	Int32	the register resource
-value	Uns64	the value to write to register

11.2.20 mipsWriteTLBEntry
Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

Table 23. mipsWriteTLBEntry command arguments

Argument	Type	Description
-hi0	Uns64	the TLB entry high address
-index	Uns64	the TLB entry index
-lo0	Uns64	the TLB entry low address 0
-lo1	Uns64	the TLB entry low address 1
-mask	Uns64	the TLB entry mask

12 Registers

12.1 Level 1: CMP
No registers.

12.2 Level 2: CPU

12.2.1 Core

Table 24. Registers at level 2, type: CPU, register group: 'Core'

Name	Bits	Initial value (Hex)		Description

zero	32	0	r-	constant zero
at	32	0	rw	
v0	32	0	rw	
v1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
t0	32	0	rw	
t1	32	0	rw	
t2	32	0	rw	
t3	32	0	rw	
t4	32	0	rw	
t5	32	0	rw	
t6	32	0	rw	
t7	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
s2	32	0	rw	
s3	32	0	rw	
s4	32	0	rw	
s5	32	0	rw	
s6	32	0	rw	
s7	32	0	rw	
t8	32	0	rw	
t9	32	0	rw	
k0	32	0	rw	
k1	32	0	rw	
gp	32	0	rw	
sp	32	0	rw	stack pointer
s8	32	0	rw	frame pointer
ra	32	0	rw	
pc	32	bfc00000	rw	program counter

12.2.2 FPU

Table 25. Registers at level 2, type: CPU, register group: 'FPU'

Name	Bits	Initial value (Hex)		Description
f0	32	0	rw	
f1	32	0	rw	
f2	32	0	rw	
f3	32	0	rw	

f4	32	0	rw	
f5	32	0	rw	
f6	32	0	rw	
f7	32	0	rw	
f8	32	0	rw	
f9	32	0	rw	
f10	32	0	rw	
f11	32	0	rw	
f12	32	0	rw	
f13	32	0	rw	
f14	32	0	rw	
f15	32	0	rw	
f16	32	0	rw	
f17	32	0	rw	
f18	32	0	rw	
f19	32	0	rw	
f20	32	0	rw	
f21	32	0	rw	
f22	32	0	rw	
f23	32	0	rw	
f24	32	0	rw	
f25	32	0	rw	
f26	32	0	rw	
f27	32	0	rw	
f28	32	0	rw	
f29	32	0	rw	
f30	32	0	rw	
f31	32	0	rw	
fsr	32	c0000	rw	floating point status
fir	32	30f30320	r-	floating point information

12.2.3 DSP

Table 26. Registers at level 2, type: CPU, register group: 'DSP'

Name	Bits	Initial value (Hex)		Description
lo	32	0	rw	
hi	32	0	rw	
lo1	32	0	rw	
hi1	32	0	rw	
lo2	32	0	rw	
hi2	32	0	rw	
lo3	32	0	rw	

hi3	32	0	rw	
dspctl	32	0	rw	DSP control

12.2.4 Shadow

Table 27. Registers at level 2, type: CPU, register group: 'Shadow'

Name	Bits	Initial value (Hex)		Description
zero[0]	32	0	r-	constant zero
at[0]	32	0	rw	
v0[0]	32	0	rw	
v1[0]	32	0	rw	
a0[0]	32	0	rw	
a1[0]	32	0	rw	
a2[0]	32	0	rw	
a3[0]	32	0	rw	
t0[0]	32	0	rw	
t1[0]	32	0	rw	
t2[0]	32	0	rw	
t3[0]	32	0	rw	
t4[0]	32	0	rw	
t5[0]	32	0	rw	
t6[0]	32	0	rw	
t7[0]	32	0	rw	
s0[0]	32	0	rw	
s1[0]	32	0	rw	
s2[0]	32	0	rw	
s3[0]	32	0	rw	
s4[0]	32	0	rw	
s5[0]	32	0	rw	
s6[0]	32	0	rw	
s7[0]	32	0	rw	
t8[0]	32	0	rw	
t9[0]	32	0	rw	
k0[0]	32	0	rw	
k1[0]	32	0	rw	
gp[0]	32	0	rw	
sp[0]	32	0	rw	stack pointer
s8[0]	32	0	rw	frame pointer
ra[0]	32	0	rw	

12.2.5 COP0

Table 28. Registers at level 2, type: CPU, register group: 'COP0'

Name	Bits	Initial value (Hex)		Description
sr	32	400004	rw	CP0 register 12/0
bad	64	0	rw	CP0 register 8/0
cause	32	0	rw	CP0 register 13/0
index	32	0	rw	CP0 register 0/0
random	32	0	rw	CP0 register 1/0
entrylo0	64	0	rw	CP0 register 2/0
entrylo1	64	0	rw	CP0 register 3/0
context	32	0	rw	CP0 register 4/0
contextconfig	32	7ffff0	rw	CP0 register 4/1
userlocal	32	0	rw	CP0 register 4/2
pagemask	32	0	rw	CP0 register 5/0
pagegrain	32	0	rw	CP0 register 5/1
segctl0	32	200010	rw	CP0 register 5/2
segctl1	32	30002	rw	CP0 register 5/3
segctl2	32	380438	rw	CP0 register 5/4
pwbase	32	0	rw	CP0 register 5/5
pwfield	32	c30c302	rw	CP0 register 5/6
pwsize	32	40	rw	CP0 register 5/7
wired	32	0	rw	CP0 register 6/0
pwctl	32	0	rw	CP0 register 6/6
hwrena	32	0	rw	CP0 register 7/0
badvaddr	64	0	rw	CP0 register 8/0
badinstr	32	0	rw	CP0 register 8/1
badinstrp	32	0	rw	CP0 register 8/2
count	32	0	rw	CP0 register 9/0
entryhi	64	0	rw	CP0 register 10/0
guestctl1	32	0	rw	CP0 register 10/4
guestctl2	32	0	rw	CP0 register 10/5
guestctl3	32	0	rw	CP0 register 10/6
compare	32	0	rw	CP0 register 11/0
guestctl0ext	32	40	rw	CP0 register 11/4
status	32	400004	rw	CP0 register 12/0
intctl	32	ff800000	rw	CP0 register 12/1
srsctl	32	0	rw	CP0 register 12/2
srsmap	32	0	rw	CP0 register 12/3
guestctl0	32	c4c00fc	rw	CP0 register 12/6
gtoffset	32	0	rw	CP0 register 12/7
epc	32	0	rw	CP0 register 14/0
prid	32	1a800	rw	CP0 register 15/0
ebase	32	80000000	rw	CP0 register 15/1

cdmmbase	32	0	rw	CP0 register 15/2
cmgcrbase	32	1fbf800	rw	CP0 register 15/3
config	32	80048482	rw	CP0 register 16/0
config1	32	fea35193	rw	CP0 register 16/1
config2	32	80000000	rw	CP0 register 16/2
config3	32	bf8032a8	rw	CP0 register 16/3
config4	32	c01c0000	rw	CP0 register 16/4
config5	32	10000038	rw	CP0 register 16/5
config6	32	0	rw	CP0 register 16/6
config7	32	80054c20	rw	CP0 register 16/7
lladdr	32	0	rw	CP0 register 17/0
maar	32	0	rw	CP0 register 17/1
maari	32	0	rw	CP0 register 17/2
debug	32	2030000	rw	CP0 register 23/0
depc	32	0	rw	CP0 register 24/0
perfctl0	32	80000000	rw	CP0 register 25/0
perfcnt0	32	0	rw	CP0 register 25/1
perfctl1	32	80000000	rw	CP0 register 25/2
perfcnt1	32	0	rw	CP0 register 25/3
perfctl2	32	80000000	rw	CP0 register 25/4
perfcnt2	32	0	rw	CP0 register 25/5
perfctl3	32	0	rw	CP0 register 25/6
perfcnt3	32	0	rw	CP0 register 25/7
errctl	32	0	rw	CP0 register 26/0
itaglo	64	0	rw	CP0 register 28/0
idatalo	32	0	rw	CP0 register 28/1
dtaglo	64	0	rw	CP0 register 28/2
ddatalo	32	0	rw	CP0 register 28/3
l23taglo	32	0	rw	CP0 register 28/4
l23datalo	32	0	rw	CP0 register 28/5
itaghi	32	0	rw	CP0 register 29/0
idatahi	32	0	rw	CP0 register 29/1
l23datahi	32	0	rw	CP0 register 29/5
errorepc	32	0	rw	CP0 register 30/0
desave	32	0	rw	CP0 register 31/0
kscratch1	32	0	rw	CP0 register 31/2
kscratch2	32	0	rw	CP0 register 31/3
kscratch3	32	0	rw	CP0 register 31/4
guestindex	32	0	rw	CP0 guest register 0/0
guestrandom	32	0	rw	CP0 guest register 1/0
guestentrylo0	64	0	rw	CP0 guest register 2/0
guestentrylo1	64	0	rw	CP0 guest register 3/0

guestcontext	32	0	rw	CP0 guest register 4/0
guestcontextconfig	32	7ffff0	rw	CP0 guest register 4/1
guestuserlocal	32	0	rw	CP0 guest register 4/2
guestpagemask	32	0	rw	CP0 guest register 5/0
guestpagegrain	32	0	rw	CP0 guest register 5/1
guestsegctl0	32	200010	rw	CP0 guest register 5/2
guestsegctl1	32	30002	rw	CP0 guest register 5/3
guestsegctl2	32	380438	rw	CP0 guest register 5/4
guestpwbase	32	0	rw	CP0 guest register 5/5
guestpwfield	32	c30c302	rw	CP0 guest register 5/6
guestpwsize	32	40	rw	CP0 guest register 5/7
guestwired	32	0	rw	CP0 guest register 6/0
guestpwctl	32	0	rw	CP0 guest register 6/6
guesthwrena	32	0	rw	CP0 guest register 7/0
guestbadvaddr	64	0	rw	CP0 guest register 8/0
guestbadinstr	32	0	rw	CP0 guest register 8/1
guestbadinstrp	32	0	rw	CP0 guest register 8/2
guestcount	32	0	rw	CP0 guest register 9/0
guestentryhi	64	0	rw	CP0 guest register 10/0
guestguestctl1	32	0	rw	CP0 guest register 10/4
guestguestctl2	32	0	rw	CP0 guest register 10/5
guestguestctl3	32	0	rw	CP0 guest register 10/6
guestcompare	32	0	rw	CP0 guest register 11/0
guestguestctl0ext	32	0	rw	CP0 guest register 11/4
gueststatus	32	400004	rw	CP0 guest register 12/0
guestintctl	32	fc000000	rw	CP0 guest register 12/1
guestsrsctl	32	0	rw	CP0 guest register 12/2
guestsrsmap	32	0	rw	CP0 guest register 12/3
guestguestctl0	32	0	rw	CP0 guest register 12/6
guestgtoffset	32	0	rw	CP0 guest register 12/7
guestcause	32	0	rw	CP0 guest register 13/0
guestepc	32	0	rw	CP0 guest register 14/0
guestprid	32	0	rw	CP0 guest register 15/0
guestebase	32	80000000	rw	CP0 guest register 15/1
guestcdmmbase	32	0	rw	CP0 guest register 15/2
guestcmgcrbase	32	0	rw	CP0 guest register 15/3
guestconfig	32	80048482	rw	CP0 guest register 16/0
guestconfig1	32	fea35191	rw	CP0 guest register 16/1
guestconfig2	32	80007000	rw	CP0 guest register 16/2
guestconfig3	32	9f003220	rw	CP0 guest register 16/3
guestconfig4	32	c01c0000	rw	CP0 guest register 16/4
guestconfig5	32	10000038	rw	CP0 guest register 16/5

guestconfig6	32	0	rw	CP0 guest register 16/6
guestconfig7	32	0	rw	CP0 guest register 16/7
guestlladdr	32	0	rw	CP0 guest register 17/0
guestmaar	32	0	rw	CP0 guest register 17/1
guestmaari	32	0	rw	CP0 guest register 17/2
guestdebug	32	0	rw	CP0 guest register 23/0
guestdepc	32	0	rw	CP0 guest register 24/0
guestperfctl0	32	80000000	rw	CP0 guest register 25/0
guestperfcnt0	32	0	rw	CP0 guest register 25/1
guestperfctl1	32	80000000	rw	CP0 guest register 25/2
guestperfcnt1	32	0	rw	CP0 guest register 25/3
guestperfctl2	32	80000000	rw	CP0 guest register 25/4
guestperfcnt2	32	0	rw	CP0 guest register 25/5
guestperfctl3	32	0	rw	CP0 guest register 25/6
guestperfcnt3	32	0	rw	CP0 guest register 25/7
guesterrctl	32	0	rw	CP0 guest register 26/0
guestitaglo	64	0	rw	CP0 guest register 28/0
guestidatalo	32	0	rw	CP0 guest register 28/1
guestdtaglo	64	0	rw	CP0 guest register 28/2
guestddatalo	32	0	rw	CP0 guest register 28/3
guestl23taglo	32	0	rw	CP0 guest register 28/4
guestl23datalo	32	0	rw	CP0 guest register 28/5
guestitaghi	32	0	rw	CP0 guest register 29/0
guestidatahi	32	0	rw	CP0 guest register 29/1
guestl23datahi	32	0	rw	CP0 guest register 29/5
guesterrorepc	32	0	rw	CP0 guest register 30/0
guestdesave	32	0	rw	CP0 guest register 31/0
guestkscratch1	32	0	rw	CP0 guest register 31/2
guestkscratch2	32	0	rw	CP0 guest register 31/3
guestkscratch3	32	0	rw	CP0 guest register 31/4

12.2.6 MSA

Table 29. Registers at level 2, type: CPU, register group: 'MSA'

Name	Bits	Initial value (Hex)		Description
w0	128	-	rw	
w1	128	-	rw	
w2	128	-	rw	
w3	128	-	rw	
w4	128	-	rw	
w5	128	-	rw	
w6	128	-	rw	
w7	128	-	rw	

w8	128	-	rw	
w9	128	-	rw	
w10	128	-	rw	
w11	128	-	rw	
w12	128	-	rw	
w13	128	-	rw	
w14	128	-	rw	
w15	128	-	rw	
w16	128	-	rw	
w17	128	-	rw	
w18	128	-	rw	
w19	128	-	rw	
w20	128	-	rw	
w21	128	-	rw	
w22	128	-	rw	
w23	128	-	rw	
w24	128	-	rw	
w25	128	-	rw	
w26	128	-	rw	
w27	128	-	rw	
w28	128	-	rw	
w29	128	-	rw	
w30	128	-	rw	
w31	128	-	rw	
msair	32	320	r-	MSA implementation
msacsr	32	0	rw	MSA control and status
msaaccess	32	-	r-	MSA access
msasave	32	-	r-	MSA save
msamodify	32	-	r-	MSA modify
msarequest	32	-	r-	MSA request
msamap	32	-	r-	MSA map
msaunmap	32	-	r-	MSA unmap

12.2.7 CMP_GCR

Table 30. Registers at level 2, type: CPU, register group: 'CMP_GCR'

Name	Bits	Initial value (Hex)		Description
GCR_CONFIG	32	3	r-	
GCR_BASE	32	1fbf8000	rw	
GCR_BASE_UPPER	32	0	rw	
GCR_CONTROL	32	10000	rw	
GCR_ACCESS	32	ff	rw	

GCR_REV	32	0	r-	
GCR_ERROR_MASK	32	0	rw	
GCR_ERROR_CAUSE	32	0	rw	
GCR_ERROR_ADDR	32	0	rw	
GCR_ERROR_ADDR_UPPER	32	0	rw	
GCR_ERROR_MULT	32	0	rw	
GCR_CUSTOM_BASE	32	0	rw	
GCR_CUSTOM_BASE_UPPER	32	0	rw	
GCR_CUSTOM_STATUS	32	0	r-	
GCR_GIC_BASE	32	0	rw	
GCR_GIC_BASE_UPPER	32	0	rw	
GCR_CPC_BASE	32	0	rw	
GCR_CPC_BASE_UPPER	32	0	rw	
GCR_GIC_STATUS	32	1	r-	
GCR_CACHE_REV	32	0	r-	
GCR_CPC_STATUS	32	1	r-	
GCR_L2_CONFIG	32	0	rw	
GCR_SYS_CONFIG2	32	0	r-	
GCR_IOCU1_REV	32	0	r-	
GCR_CL_RESET_RELEASE	32	0	-w	
GCR_CL_COHERENCE	32	0	rw	
GCR_CL_CONFIG	32	0	r-	
GCR_CL_OTHER	32	0	rw	
GCR_CL_RESET_BASE	32	bfc00000	rw	
GCR_CL_ID	32	0	r-	
GCR_CL_RESET_EXT_BASE	32	40000001	rw	
GCR_CO_RESET_RELEASE	32	0	-w	
GCR_CO_COHERENCE	32	0	rw	
GCR_CO_CONFIG	32	0	r-	
GCR_CO_OTHER	32	0	rw	
GCR_CO_RESET_BASE	32	bfc00000	rw	
GCR_CO_ID	32	0	r-	
GCR_CO_RESET_EXT_BASE	32	40000001	rw	

12.2.8 CMP_CPC

Table 31. Registers at level 2, type: CPU, register group: 'CMP_CPC'

Name	Bits	Initial value (Hex)		Description
CPC_ACCESS	32	ff	rw	
CPC_SEQDEL	32	0	rw	
CPC_RAIL	32	0	rw	
CPC_RESETLEN	32	0	rw	

CPC_REVISION	32	0	r-	
CPC_CMD	32	0	rw	
CPC_STAT_CONF	32	300200	rw	
CPC_OTHER	32	0	rw	
CPC_CMD	32	0	rw	
CPC_STAT_CONF	32	300200	rw	
CPC_OTHER	32	0	rw	

12.2.9 CMP_GIC

Table 32. Registers at level 2, type: CPU, register group: 'CMP_GIC'

Name	Bits	Initial value (Hex)		Description
GIC_SH_CONFIG	32	8040003	rw	
GIC_CounterLo	32	0	rw	
GIC_CounterHi	32	0	rw	
GIC_SH_REVISION	32	0	r-	
GIC_SH_POL31_0	32	0	rw	
GIC_SH_POL63_32	32	0	rw	
GIC_SH_POL95_64	32	0	rw	
GIC_SH_POL127_96	32	0	rw	
GIC_SH_POL159_128	32	0	rw	
GIC_SH_POL191_160	32	0	rw	
GIC_SH_POL223_192	32	0	rw	
GIC_SH_POL255_224	32	0	rw	
GIC_SH_TRIG31_0	32	0	rw	
GIC_SH_TRIG63_32	32	0	rw	
GIC_SH_TRIG95_64	32	0	rw	
GIC_SH_TRIG127_96	32	0	rw	
GIC_SH_TRIG159_128	32	0	rw	
GIC_SH_TRIG191_160	32	0	rw	
GIC_SH_TRIG223_192	32	0	rw	
GIC_SH_TRIG255_224	32	0	rw	
GIC_SH_DUAL31_0	32	0	rw	
GIC_SH_DUAL63_32	32	0	rw	
GIC_SH_DUAL95_64	32	0	rw	
GIC_SH_DUAL127_96	32	0	rw	
GIC_SH_DUAL159_128	32	0	rw	
GIC_SH_DUAL191_160	32	0	rw	
GIC_SH_DUAL223_192	32	0	rw	
GIC_SH_DUAL255_224	32	0	rw	
GIC_SH_WEDGE	32	0	-w	
GIC_SH_RMASK31_0	32	0	-w	

GIC_SH_RMASK63_32	32	0	-w	
GIC_SH_RMASK95_64	32	0	-w	
GIC_SH_RMASK127_96	32	0	-w	
GIC_SH_RMASK159_128	32	0	-w	
GIC_SH_RMASK191_160	32	0	-w	
GIC_SH_RMASK223_192	32	0	-w	
GIC_SH_RMASK255_224	32	0	-w	
GIC_SH_SMASK31_0	32	0	-w	
GIC_SH_SMASK63_32	32	0	-w	
GIC_SH_SMASK95_64	32	0	-w	
GIC_SH_SMASK127_96	32	0	-w	
GIC_SH_SMASK159_128	32	0	-w	
GIC_SH_SMASK191_160	32	0	-w	
GIC_SH_SMASK223_192	32	0	-w	
GIC_SH_SMASK255_224	32	0	-w	
GIC_SH_MASK31_0	32	0	r-	
GIC_SH_MASK63_32	32	0	r-	
GIC_SH_MASK95_64	32	0	r-	
GIC_SH_MASK127_96	32	0	r-	
GIC_SH_MASK159_128	32	0	r-	
GIC_SH_MASK191_160	32	0	r-	
GIC_SH_MASK223_192	32	0	r-	
GIC_SH_MASK255_224	32	0	r-	
GIC_SH_PEND31_0	32	0	r-	
GIC_SH_PEND63_32	32	0	r-	
GIC_SH_PEND95_64	32	0	r-	
GIC_SH_PEND127_96	32	0	r-	
GIC_SH_PEND159_128	32	0	r-	
GIC_SH_PEND191_160	32	0	r-	
GIC_SH_PEND223_192	32	0	r-	
GIC_SH_PEND255_224	32	0	r-	
GIC_SH_MAP000_PIN	32	80000000	rw	
GIC_SH_MAP001_PIN	32	80000000	rw	
GIC_SH_MAP002_PIN	32	80000000	rw	
GIC_SH_MAP003_PIN	32	80000000	rw	
GIC_SH_MAP004_PIN	32	80000000	rw	
GIC_SH_MAP005_PIN	32	80000000	rw	
GIC_SH_MAP006_PIN	32	80000000	rw	
GIC_SH_MAP007_PIN	32	80000000	rw	
GIC_SH_MAP008_PIN	32	80000000	rw	
GIC_SH_MAP009_PIN	32	80000000	rw	
GIC_SH_MAP010_PIN	32	80000000	rw	

GIC_SH_MAP011_PIN	32	80000000	rw	
GIC_SH_MAP012_PIN	32	80000000	rw	
GIC_SH_MAP013_PIN	32	80000000	rw	
GIC_SH_MAP014_PIN	32	80000000	rw	
GIC_SH_MAP015_PIN	32	80000000	rw	
GIC_SH_MAP016_PIN	32	80000000	rw	
GIC_SH_MAP017_PIN	32	80000000	rw	
GIC_SH_MAP018_PIN	32	80000000	rw	
GIC_SH_MAP019_PIN	32	80000000	rw	
GIC_SH_MAP020_PIN	32	80000000	rw	
GIC_SH_MAP021_PIN	32	80000000	rw	
GIC_SH_MAP022_PIN	32	80000000	rw	
GIC_SH_MAP023_PIN	32	80000000	rw	
GIC_SH_MAP024_PIN	32	80000000	rw	
GIC_SH_MAP025_PIN	32	80000000	rw	
GIC_SH_MAP026_PIN	32	80000000	rw	
GIC_SH_MAP027_PIN	32	80000000	rw	
GIC_SH_MAP028_PIN	32	80000000	rw	
GIC_SH_MAP029_PIN	32	80000000	rw	
GIC_SH_MAP030_PIN	32	80000000	rw	
GIC_SH_MAP031_PIN	32	80000000	rw	
GIC_SH_MAP032_PIN	32	80000000	rw	
GIC_SH_MAP033_PIN	32	80000000	rw	
GIC_SH_MAP034_PIN	32	80000000	rw	
GIC_SH_MAP035_PIN	32	80000000	rw	
GIC_SH_MAP036_PIN	32	80000000	rw	
GIC_SH_MAP037_PIN	32	80000000	rw	
GIC_SH_MAP038_PIN	32	80000000	rw	
GIC_SH_MAP039_PIN	32	80000000	rw	
GIC_SH_MAP040_PIN	32	0	rw	
GIC_SH_MAP041_PIN	32	0	rw	
GIC_SH_MAP042_PIN	32	0	rw	
GIC_SH_MAP043_PIN	32	0	rw	
GIC_SH_MAP044_PIN	32	0	rw	
GIC_SH_MAP045_PIN	32	0	rw	
GIC_SH_MAP046_PIN	32	0	rw	
GIC_SH_MAP047_PIN	32	0	rw	
GIC_SH_MAP048_PIN	32	0	rw	
GIC_SH_MAP049_PIN	32	0	rw	
GIC_SH_MAP050_PIN	32	0	rw	
GIC_SH_MAP051_PIN	32	0	rw	
GIC_SH_MAP052_PIN	32	0	rw	

GIC_SH_MAP053_PIN	32	0	rw	
GIC_SH_MAP054_PIN	32	0	rw	
GIC_SH_MAP055_PIN	32	0	rw	
GIC_SH_MAP056_PIN	32	0	rw	
GIC_SH_MAP057_PIN	32	0	rw	
GIC_SH_MAP058_PIN	32	0	rw	
GIC_SH_MAP059_PIN	32	0	rw	
GIC_SH_MAP060_PIN	32	0	rw	
GIC_SH_MAP061_PIN	32	0	rw	
GIC_SH_MAP062_PIN	32	0	rw	
GIC_SH_MAP063_PIN	32	0	rw	
GIC_SH_MAP064_PIN	32	0	rw	
GIC_SH_MAP065_PIN	32	0	rw	
GIC_SH_MAP066_PIN	32	0	rw	
GIC_SH_MAP067_PIN	32	0	rw	
GIC_SH_MAP068_PIN	32	0	rw	
GIC_SH_MAP069_PIN	32	0	rw	
GIC_SH_MAP070_PIN	32	0	rw	
GIC_SH_MAP071_PIN	32	0	rw	
GIC_SH_MAP072_PIN	32	0	rw	
GIC_SH_MAP073_PIN	32	0	rw	
GIC_SH_MAP074_PIN	32	0	rw	
GIC_SH_MAP075_PIN	32	0	rw	
GIC_SH_MAP076_PIN	32	0	rw	
GIC_SH_MAP077_PIN	32	0	rw	
GIC_SH_MAP078_PIN	32	0	rw	
GIC_SH_MAP079_PIN	32	0	rw	
GIC_SH_MAP080_PIN	32	0	rw	
GIC_SH_MAP081_PIN	32	0	rw	
GIC_SH_MAP082_PIN	32	0	rw	
GIC_SH_MAP083_PIN	32	0	rw	
GIC_SH_MAP084_PIN	32	0	rw	
GIC_SH_MAP085_PIN	32	0	rw	
GIC_SH_MAP086_PIN	32	0	rw	
GIC_SH_MAP087_PIN	32	0	rw	
GIC_SH_MAP088_PIN	32	0	rw	
GIC_SH_MAP089_PIN	32	0	rw	
GIC_SH_MAP090_PIN	32	0	rw	
GIC_SH_MAP091_PIN	32	0	rw	
GIC_SH_MAP092_PIN	32	0	rw	
GIC_SH_MAP093_PIN	32	0	rw	
GIC_SH_MAP094_PIN	32	0	rw	

GIC_SH_MAP095_PIN	32	0	rw	
GIC_SH_MAP096_PIN	32	0	rw	
GIC_SH_MAP097_PIN	32	0	rw	
GIC_SH_MAP098_PIN	32	0	rw	
GIC_SH_MAP099_PIN	32	0	rw	
GIC_SH_MAP100_PIN	32	0	rw	
GIC_SH_MAP101_PIN	32	0	rw	
GIC_SH_MAP102_PIN	32	0	rw	
GIC_SH_MAP103_PIN	32	0	rw	
GIC_SH_MAP104_PIN	32	0	rw	
GIC_SH_MAP105_PIN	32	0	rw	
GIC_SH_MAP106_PIN	32	0	rw	
GIC_SH_MAP107_PIN	32	0	rw	
GIC_SH_MAP108_PIN	32	0	rw	
GIC_SH_MAP109_PIN	32	0	rw	
GIC_SH_MAP110_PIN	32	0	rw	
GIC_SH_MAP111_PIN	32	0	rw	
GIC_SH_MAP112_PIN	32	0	rw	
GIC_SH_MAP113_PIN	32	0	rw	
GIC_SH_MAP114_PIN	32	0	rw	
GIC_SH_MAP115_PIN	32	0	rw	
GIC_SH_MAP116_PIN	32	0	rw	
GIC_SH_MAP117_PIN	32	0	rw	
GIC_SH_MAP118_PIN	32	0	rw	
GIC_SH_MAP119_PIN	32	0	rw	
GIC_SH_MAP120_PIN	32	0	rw	
GIC_SH_MAP121_PIN	32	0	rw	
GIC_SH_MAP122_PIN	32	0	rw	
GIC_SH_MAP123_PIN	32	0	rw	
GIC_SH_MAP124_PIN	32	0	rw	
GIC_SH_MAP125_PIN	32	0	rw	
GIC_SH_MAP126_PIN	32	0	rw	
GIC_SH_MAP127_PIN	32	0	rw	
GIC_SH_MAP128_PIN	32	0	rw	
GIC_SH_MAP129_PIN	32	0	rw	
GIC_SH_MAP130_PIN	32	0	rw	
GIC_SH_MAP131_PIN	32	0	rw	
GIC_SH_MAP132_PIN	32	0	rw	
GIC_SH_MAP133_PIN	32	0	rw	
GIC_SH_MAP134_PIN	32	0	rw	
GIC_SH_MAP135_PIN	32	0	rw	
GIC_SH_MAP136_PIN	32	0	rw	

GIC_SH_MAP137_PIN	32	0	rw	
GIC_SH_MAP138_PIN	32	0	rw	
GIC_SH_MAP139_PIN	32	0	rw	
GIC_SH_MAP140_PIN	32	0	rw	
GIC_SH_MAP141_PIN	32	0	rw	
GIC_SH_MAP142_PIN	32	0	rw	
GIC_SH_MAP143_PIN	32	0	rw	
GIC_SH_MAP144_PIN	32	0	rw	
GIC_SH_MAP145_PIN	32	0	rw	
GIC_SH_MAP146_PIN	32	0	rw	
GIC_SH_MAP147_PIN	32	0	rw	
GIC_SH_MAP148_PIN	32	0	rw	
GIC_SH_MAP149_PIN	32	0	rw	
GIC_SH_MAP150_PIN	32	0	rw	
GIC_SH_MAP151_PIN	32	0	rw	
GIC_SH_MAP152_PIN	32	0	rw	
GIC_SH_MAP153_PIN	32	0	rw	
GIC_SH_MAP154_PIN	32	0	rw	
GIC_SH_MAP155_PIN	32	0	rw	
GIC_SH_MAP156_PIN	32	0	rw	
GIC_SH_MAP157_PIN	32	0	rw	
GIC_SH_MAP158_PIN	32	0	rw	
GIC_SH_MAP159_PIN	32	0	rw	
GIC_SH_MAP160_PIN	32	0	rw	
GIC_SH_MAP161_PIN	32	0	rw	
GIC_SH_MAP162_PIN	32	0	rw	
GIC_SH_MAP163_PIN	32	0	rw	
GIC_SH_MAP164_PIN	32	0	rw	
GIC_SH_MAP165_PIN	32	0	rw	
GIC_SH_MAP166_PIN	32	0	rw	
GIC_SH_MAP167_PIN	32	0	rw	
GIC_SH_MAP168_PIN	32	0	rw	
GIC_SH_MAP169_PIN	32	0	rw	
GIC_SH_MAP170_PIN	32	0	rw	
GIC_SH_MAP171_PIN	32	0	rw	
GIC_SH_MAP172_PIN	32	0	rw	
GIC_SH_MAP173_PIN	32	0	rw	
GIC_SH_MAP174_PIN	32	0	rw	
GIC_SH_MAP175_PIN	32	0	rw	
GIC_SH_MAP176_PIN	32	0	rw	
GIC_SH_MAP177_PIN	32	0	rw	
GIC_SH_MAP178_PIN	32	0	rw	

GIC_SH_MAP179_PIN	32	0	rw	
GIC_SH_MAP180_PIN	32	0	rw	
GIC_SH_MAP181_PIN	32	0	rw	
GIC_SH_MAP182_PIN	32	0	rw	
GIC_SH_MAP183_PIN	32	0	rw	
GIC_SH_MAP184_PIN	32	0	rw	
GIC_SH_MAP185_PIN	32	0	rw	
GIC_SH_MAP186_PIN	32	0	rw	
GIC_SH_MAP187_PIN	32	0	rw	
GIC_SH_MAP188_PIN	32	0	rw	
GIC_SH_MAP189_PIN	32	0	rw	
GIC_SH_MAP190_PIN	32	0	rw	
GIC_SH_MAP191_PIN	32	0	rw	
GIC_SH_MAP192_PIN	32	0	rw	
GIC_SH_MAP193_PIN	32	0	rw	
GIC_SH_MAP194_PIN	32	0	rw	
GIC_SH_MAP195_PIN	32	0	rw	
GIC_SH_MAP196_PIN	32	0	rw	
GIC_SH_MAP197_PIN	32	0	rw	
GIC_SH_MAP198_PIN	32	0	rw	
GIC_SH_MAP199_PIN	32	0	rw	
GIC_SH_MAP200_PIN	32	0	rw	
GIC_SH_MAP201_PIN	32	0	rw	
GIC_SH_MAP202_PIN	32	0	rw	
GIC_SH_MAP203_PIN	32	0	rw	
GIC_SH_MAP204_PIN	32	0	rw	
GIC_SH_MAP205_PIN	32	0	rw	
GIC_SH_MAP206_PIN	32	0	rw	
GIC_SH_MAP207_PIN	32	0	rw	
GIC_SH_MAP208_PIN	32	0	rw	
GIC_SH_MAP209_PIN	32	0	rw	
GIC_SH_MAP210_PIN	32	0	rw	
GIC_SH_MAP211_PIN	32	0	rw	
GIC_SH_MAP212_PIN	32	0	rw	
GIC_SH_MAP213_PIN	32	0	rw	
GIC_SH_MAP214_PIN	32	0	rw	
GIC_SH_MAP215_PIN	32	0	rw	
GIC_SH_MAP216_PIN	32	0	rw	
GIC_SH_MAP217_PIN	32	0	rw	
GIC_SH_MAP218_PIN	32	0	rw	
GIC_SH_MAP219_PIN	32	0	rw	
GIC_SH_MAP220_PIN	32	0	rw	

GIC_SH_MAP221_PIN	32	0	rw	
GIC_SH_MAP222_PIN	32	0	rw	
GIC_SH_MAP223_PIN	32	0	rw	
GIC_SH_MAP224_PIN	32	0	rw	
GIC_SH_MAP225_PIN	32	0	rw	
GIC_SH_MAP226_PIN	32	0	rw	
GIC_SH_MAP227_PIN	32	0	rw	
GIC_SH_MAP228_PIN	32	0	rw	
GIC_SH_MAP229_PIN	32	0	rw	
GIC_SH_MAP230_PIN	32	0	rw	
GIC_SH_MAP231_PIN	32	0	rw	
GIC_SH_MAP232_PIN	32	0	rw	
GIC_SH_MAP233_PIN	32	0	rw	
GIC_SH_MAP234_PIN	32	0	rw	
GIC_SH_MAP235_PIN	32	0	rw	
GIC_SH_MAP236_PIN	32	0	rw	
GIC_SH_MAP237_PIN	32	0	rw	
GIC_SH_MAP238_PIN	32	0	rw	
GIC_SH_MAP239_PIN	32	0	rw	
GIC_SH_MAP240_PIN	32	0	rw	
GIC_SH_MAP241_PIN	32	0	rw	
GIC_SH_MAP242_PIN	32	0	rw	
GIC_SH_MAP243_PIN	32	0	rw	
GIC_SH_MAP244_PIN	32	0	rw	
GIC_SH_MAP245_PIN	32	0	rw	
GIC_SH_MAP246_PIN	32	0	rw	
GIC_SH_MAP247_PIN	32	0	rw	
GIC_SH_MAP248_PIN	32	0	rw	
GIC_SH_MAP249_PIN	32	0	rw	
GIC_SH_MAP250_PIN	32	0	rw	
GIC_SH_MAP251_PIN	32	0	rw	
GIC_SH_MAP252_PIN	32	0	rw	
GIC_SH_MAP253_PIN	32	0	rw	
GIC_SH_MAP254_PIN	32	0	rw	
GIC_SH_MAP255_PIN	32	0	rw	
GIC_SH_MAP000_VPE31_0	32	0	rw	
GIC_SH_MAP001_VPE31_0	32	0	rw	
GIC_SH_MAP002_VPE31_0	32	0	rw	
GIC_SH_MAP003_VPE31_0	32	0	rw	
GIC_SH_MAP004_VPE31_0	32	0	rw	
GIC_SH_MAP005_VPE31_0	32	0	rw	
GIC_SH_MAP006_VPE31_0	32	0	rw	

GIC_SH_MAP007_VPE31_0	32	0	rw	
GIC_SH_MAP008_VPE31_0	32	0	rw	
GIC_SH_MAP009_VPE31_0	32	0	rw	
GIC_SH_MAP010_VPE31_0	32	0	rw	
GIC_SH_MAP011_VPE31_0	32	0	rw	
GIC_SH_MAP012_VPE31_0	32	0	rw	
GIC_SH_MAP013_VPE31_0	32	0	rw	
GIC_SH_MAP014_VPE31_0	32	0	rw	
GIC_SH_MAP015_VPE31_0	32	0	rw	
GIC_SH_MAP016_VPE31_0	32	0	rw	
GIC_SH_MAP017_VPE31_0	32	0	rw	
GIC_SH_MAP018_VPE31_0	32	0	rw	
GIC_SH_MAP019_VPE31_0	32	0	rw	
GIC_SH_MAP020_VPE31_0	32	0	rw	
GIC_SH_MAP021_VPE31_0	32	0	rw	
GIC_SH_MAP022_VPE31_0	32	0	rw	
GIC_SH_MAP023_VPE31_0	32	0	rw	
GIC_SH_MAP024_VPE31_0	32	0	rw	
GIC_SH_MAP025_VPE31_0	32	0	rw	
GIC_SH_MAP026_VPE31_0	32	0	rw	
GIC_SH_MAP027_VPE31_0	32	0	rw	
GIC_SH_MAP028_VPE31_0	32	0	rw	
GIC_SH_MAP029_VPE31_0	32	0	rw	
GIC_SH_MAP030_VPE31_0	32	0	rw	
GIC_SH_MAP031_VPE31_0	32	0	rw	
GIC_SH_MAP032_VPE31_0	32	0	rw	
GIC_SH_MAP033_VPE31_0	32	0	rw	
GIC_SH_MAP034_VPE31_0	32	0	rw	
GIC_SH_MAP035_VPE31_0	32	0	rw	
GIC_SH_MAP036_VPE31_0	32	0	rw	
GIC_SH_MAP037_VPE31_0	32	0	rw	
GIC_SH_MAP038_VPE31_0	32	0	rw	
GIC_SH_MAP039_VPE31_0	32	0	rw	
GIC_SH_MAP040_VPE31_0	32	0	rw	
GIC_SH_MAP041_VPE31_0	32	0	rw	
GIC_SH_MAP042_VPE31_0	32	0	rw	
GIC_SH_MAP043_VPE31_0	32	0	rw	
GIC_SH_MAP044_VPE31_0	32	0	rw	
GIC_SH_MAP045_VPE31_0	32	0	rw	
GIC_SH_MAP046_VPE31_0	32	0	rw	
GIC_SH_MAP047_VPE31_0	32	0	rw	
GIC_SH_MAP048_VPE31_0	32	0	rw	

GIC_SH_MAP049_VPE31_0	32	0	rw	
GIC_SH_MAP050_VPE31_0	32	0	rw	
GIC_SH_MAP051_VPE31_0	32	0	rw	
GIC_SH_MAP052_VPE31_0	32	0	rw	
GIC_SH_MAP053_VPE31_0	32	0	rw	
GIC_SH_MAP054_VPE31_0	32	0	rw	
GIC_SH_MAP055_VPE31_0	32	0	rw	
GIC_SH_MAP056_VPE31_0	32	0	rw	
GIC_SH_MAP057_VPE31_0	32	0	rw	
GIC_SH_MAP058_VPE31_0	32	0	rw	
GIC_SH_MAP059_VPE31_0	32	0	rw	
GIC_SH_MAP060_VPE31_0	32	0	rw	
GIC_SH_MAP061_VPE31_0	32	0	rw	
GIC_SH_MAP062_VPE31_0	32	0	rw	
GIC_SH_MAP063_VPE31_0	32	0	rw	
GIC_SH_MAP064_VPE31_0	32	0	rw	
GIC_SH_MAP065_VPE31_0	32	0	rw	
GIC_SH_MAP066_VPE31_0	32	0	rw	
GIC_SH_MAP067_VPE31_0	32	0	rw	
GIC_SH_MAP068_VPE31_0	32	0	rw	
GIC_SH_MAP069_VPE31_0	32	0	rw	
GIC_SH_MAP070_VPE31_0	32	0	rw	
GIC_SH_MAP071_VPE31_0	32	0	rw	
GIC_SH_MAP072_VPE31_0	32	0	rw	
GIC_SH_MAP073_VPE31_0	32	0	rw	
GIC_SH_MAP074_VPE31_0	32	0	rw	
GIC_SH_MAP075_VPE31_0	32	0	rw	
GIC_SH_MAP076_VPE31_0	32	0	rw	
GIC_SH_MAP077_VPE31_0	32	0	rw	
GIC_SH_MAP078_VPE31_0	32	0	rw	
GIC_SH_MAP079_VPE31_0	32	0	rw	
GIC_SH_MAP080_VPE31_0	32	0	rw	
GIC_SH_MAP081_VPE31_0	32	0	rw	
GIC_SH_MAP082_VPE31_0	32	0	rw	
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GIC_SH_MAP084_VPE31_0	32	0	rw	
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GIC_SH_MAP086_VPE31_0	32	0	rw	
GIC_SH_MAP087_VPE31_0	32	0	rw	
GIC_SH_MAP088_VPE31_0	32	0	rw	
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GIC_SH_MAP090_VPE31_0	32	0	rw	

GIC_SH_MAP091_VPE31_0	32	0	rw	
GIC_SH_MAP092_VPE31_0	32	0	rw	
GIC_SH_MAP093_VPE31_0	32	0	rw	
GIC_SH_MAP094_VPE31_0	32	0	rw	
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GIC_SH_MAP096_VPE31_0	32	0	rw	
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GIC_SH_MAP098_VPE31_0	32	0	rw	
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GIC_SH_MAP104_VPE31_0	32	0	rw	
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GIC_SH_MAP108_VPE31_0	32	0	rw	
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GIC_SH_MAP110_VPE31_0	32	0	rw	
GIC_SH_MAP111_VPE31_0	32	0	rw	
GIC_SH_MAP112_VPE31_0	32	0	rw	
GIC_SH_MAP113_VPE31_0	32	0	rw	
GIC_SH_MAP114_VPE31_0	32	0	rw	
GIC_SH_MAP115_VPE31_0	32	0	rw	
GIC_SH_MAP116_VPE31_0	32	0	rw	
GIC_SH_MAP117_VPE31_0	32	0	rw	
GIC_SH_MAP118_VPE31_0	32	0	rw	
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GIC_SH_MAP123_VPE31_0	32	0	rw	
GIC_SH_MAP124_VPE31_0	32	0	rw	
GIC_SH_MAP125_VPE31_0	32	0	rw	
GIC_SH_MAP126_VPE31_0	32	0	rw	
GIC_SH_MAP127_VPE31_0	32	0	rw	
GIC_SH_MAP128_VPE31_0	32	0	rw	
GIC_SH_MAP129_VPE31_0	32	0	rw	
GIC_SH_MAP130_VPE31_0	32	0	rw	
GIC_SH_MAP131_VPE31_0	32	0	rw	
GIC_SH_MAP132_VPE31_0	32	0	rw	

GIC_SH_MAP133_VPE31_0	32	0	rw	
GIC_SH_MAP134_VPE31_0	32	0	rw	
GIC_SH_MAP135_VPE31_0	32	0	rw	
GIC_SH_MAP136_VPE31_0	32	0	rw	
GIC_SH_MAP137_VPE31_0	32	0	rw	
GIC_SH_MAP138_VPE31_0	32	0	rw	
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GIC_SH_MAP142_VPE31_0	32	0	rw	
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GIC_SH_MAP144_VPE31_0	32	0	rw	
GIC_SH_MAP145_VPE31_0	32	0	rw	
GIC_SH_MAP146_VPE31_0	32	0	rw	
GIC_SH_MAP147_VPE31_0	32	0	rw	
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GIC_SH_MAP150_VPE31_0	32	0	rw	
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GIC_SH_MAP162_VPE31_0	32	0	rw	
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GIC_SH_MAP164_VPE31_0	32	0	rw	
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GIC_SH_MAP166_VPE31_0	32	0	rw	
GIC_SH_MAP167_VPE31_0	32	0	rw	
GIC_SH_MAP168_VPE31_0	32	0	rw	
GIC_SH_MAP169_VPE31_0	32	0	rw	
GIC_SH_MAP170_VPE31_0	32	0	rw	
GIC_SH_MAP171_VPE31_0	32	0	rw	
GIC_SH_MAP172_VPE31_0	32	0	rw	
GIC_SH_MAP173_VPE31_0	32	0	rw	
GIC_SH_MAP174_VPE31_0	32	0	rw	

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GIC_SH_MAP177_VPE31_0	32	0	rw	
GIC_SH_MAP178_VPE31_0	32	0	rw	
GIC_SH_MAP179_VPE31_0	32	0	rw	
GIC_SH_MAP180_VPE31_0	32	0	rw	
GIC_SH_MAP181_VPE31_0	32	0	rw	
GIC_SH_MAP182_VPE31_0	32	0	rw	
GIC_SH_MAP183_VPE31_0	32	0	rw	
GIC_SH_MAP184_VPE31_0	32	0	rw	
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GIC_SH_MAP186_VPE31_0	32	0	rw	
GIC_SH_MAP187_VPE31_0	32	0	rw	
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GIC_SH_MAP199_VPE31_0	32	0	rw	
GIC_SH_MAP200_VPE31_0	32	0	rw	
GIC_SH_MAP201_VPE31_0	32	0	rw	
GIC_SH_MAP202_VPE31_0	32	0	rw	
GIC_SH_MAP203_VPE31_0	32	0	rw	
GIC_SH_MAP204_VPE31_0	32	0	rw	
GIC_SH_MAP205_VPE31_0	32	0	rw	
GIC_SH_MAP206_VPE31_0	32	0	rw	
GIC_SH_MAP207_VPE31_0	32	0	rw	
GIC_SH_MAP208_VPE31_0	32	0	rw	
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GIC_SH_MAP210_VPE31_0	32	0	rw	
GIC_SH_MAP211_VPE31_0	32	0	rw	
GIC_SH_MAP212_VPE31_0	32	0	rw	
GIC_SH_MAP213_VPE31_0	32	0	rw	
GIC_SH_MAP214_VPE31_0	32	0	rw	
GIC_SH_MAP215_VPE31_0	32	0	rw	
GIC_SH_MAP216_VPE31_0	32	0	rw	

GIC_SH_MAP217_VPE31_0	32	0	rw	
GIC_SH_MAP218_VPE31_0	32	0	rw	
GIC_SH_MAP219_VPE31_0	32	0	rw	
GIC_SH_MAP220_VPE31_0	32	0	rw	
GIC_SH_MAP221_VPE31_0	32	0	rw	
GIC_SH_MAP222_VPE31_0	32	0	rw	
GIC_SH_MAP223_VPE31_0	32	0	rw	
GIC_SH_MAP224_VPE31_0	32	0	rw	
GIC_SH_MAP225_VPE31_0	32	0	rw	
GIC_SH_MAP226_VPE31_0	32	0	rw	
GIC_SH_MAP227_VPE31_0	32	0	rw	
GIC_SH_MAP228_VPE31_0	32	0	rw	
GIC_SH_MAP229_VPE31_0	32	0	rw	
GIC_SH_MAP230_VPE31_0	32	0	rw	
GIC_SH_MAP231_VPE31_0	32	0	rw	
GIC_SH_MAP232_VPE31_0	32	0	rw	
GIC_SH_MAP233_VPE31_0	32	0	rw	
GIC_SH_MAP234_VPE31_0	32	0	rw	
GIC_SH_MAP235_VPE31_0	32	0	rw	
GIC_SH_MAP236_VPE31_0	32	0	rw	
GIC_SH_MAP237_VPE31_0	32	0	rw	
GIC_SH_MAP238_VPE31_0	32	0	rw	
GIC_SH_MAP239_VPE31_0	32	0	rw	
GIC_SH_MAP240_VPE31_0	32	0	rw	
GIC_SH_MAP241_VPE31_0	32	0	rw	
GIC_SH_MAP242_VPE31_0	32	0	rw	
GIC_SH_MAP243_VPE31_0	32	0	rw	
GIC_SH_MAP244_VPE31_0	32	0	rw	
GIC_SH_MAP245_VPE31_0	32	0	rw	
GIC_SH_MAP246_VPE31_0	32	0	rw	
GIC_SH_MAP247_VPE31_0	32	0	rw	
GIC_SH_MAP248_VPE31_0	32	0	rw	
GIC_SH_MAP249_VPE31_0	32	0	rw	
GIC_SH_MAP250_VPE31_0	32	0	rw	
GIC_SH_MAP251_VPE31_0	32	0	rw	
GIC_SH_MAP252_VPE31_0	32	0	rw	
GIC_SH_MAP253_VPE31_0	32	0	rw	
GIC_SH_MAP254_VPE31_0	32	0	rw	
GIC_SH_MAP255_VPE31_0	32	0	rw	
GIC_VB_DINT_SEND	32	0	-w	
GIC_VPE_CTL	32	2	rw	
GIC_VPE_PEND	32	0	r-	

GIC_VPE_MASK	32	7f	r-	
GIC_VPE_RMASK	32	0	-w	
GIC_VPE_SMASK	32	0	-w	
GIC_VPE_WD_MAP	32	40000000	rw	
GIC_VPE_COMPARE_MAP	32	80000000	rw	
GIC_VPE_TIMER_MAP	32	80000005	rw	
GIC_VPE_FDC_MAP	32	80000005	rw	
GIC_VPE_PERFCTR_MAP	32	80000005	rw	
GIC_VPE_SWInt0_MAP	32	80000000	rw	
GIC_VPE_SWInt1_MAP	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS	32	0	rw	
GIC_VPE_IDENT	32	0	r-	
GIC_VPE_WD_CONFIG	32	0	rw	
GIC_VPE_WD_COUNT	32	0	r-	
GIC_VPE_WD_INITIAL	32	0	rw	
GIC_VPE_CompareLo	32	ffffffff	rw	
GIC_VPE_CompareHi	32	ffffffff	rw	
GIC_VPE_EICSS00	32	0	rw	
GIC_VPE_EICSS01	32	0	rw	
GIC_VPE_EICSS02	32	0	rw	
GIC_VPE_EICSS03	32	0	rw	
GIC_VPE_EICSS04	32	0	rw	
GIC_VPE_EICSS05	32	0	rw	
GIC_VPE_EICSS06	32	0	rw	
GIC_VPE_EICSS07	32	0	rw	
GIC_VPE_EICSS08	32	0	rw	
GIC_VPE_EICSS09	32	0	rw	
GIC_VPE_EICSS10	32	0	rw	
GIC_VPE_EICSS11	32	0	rw	
GIC_VPE_EICSS12	32	0	rw	
GIC_VPE_EICSS13	32	0	rw	
GIC_VPE_EICSS14	32	0	rw	
GIC_VPE_EICSS15	32	0	rw	
GIC_VPE_EICSS16	32	0	rw	
GIC_VPE_EICSS17	32	0	rw	
GIC_VPE_EICSS18	32	0	rw	
GIC_VPE_EICSS19	32	0	rw	
GIC_VPE_EICSS20	32	0	rw	
GIC_VPE_EICSS21	32	0	rw	
GIC_VPE_EICSS22	32	0	rw	
GIC_VPE_EICSS23	32	0	rw	
GIC_VPE_EICSS24	32	0	rw	

GIC_VPE_EICSS25	32	0	rw	
GIC_VPE_EICSS26	32	0	rw	
GIC_VPE_EICSS27	32	0	rw	
GIC_VPE_EICSS28	32	0	rw	
GIC_VPE_EICSS29	32	0	rw	
GIC_VPE_EICSS30	32	0	rw	
GIC_VPE_EICSS31	32	0	rw	
GIC_VPE_EICSS32	32	0	rw	
GIC_VPE_EICSS33	32	0	rw	
GIC_VPE_EICSS34	32	0	rw	
GIC_VPE_EICSS35	32	0	rw	
GIC_VPE_EICSS36	32	0	rw	
GIC_VPE_EICSS37	32	0	rw	
GIC_VPE_EICSS38	32	0	rw	
GIC_VPE_EICSS39	32	0	rw	
GIC_VPE_EICSS40	32	0	rw	
GIC_VPE_EICSS41	32	0	rw	
GIC_VPE_EICSS42	32	0	rw	
GIC_VPE_EICSS43	32	0	rw	
GIC_VPE_EICSS44	32	0	rw	
GIC_VPE_EICSS45	32	0	rw	
GIC_VPE_EICSS46	32	0	rw	
GIC_VPE_EICSS47	32	0	rw	
GIC_VPE_EICSS48	32	0	rw	
GIC_VPE_EICSS49	32	0	rw	
GIC_VPE_EICSS50	32	0	rw	
GIC_VPE_EICSS51	32	0	rw	
GIC_VPE_EICSS52	32	0	rw	
GIC_VPE_EICSS53	32	0	rw	
GIC_VPE_EICSS54	32	0	rw	
GIC_VPE_EICSS55	32	0	rw	
GIC_VPE_EICSS56	32	0	rw	
GIC_VPE_EICSS57	32	0	rw	
GIC_VPE_EICSS58	32	0	rw	
GIC_VPE_EICSS59	32	0	rw	
GIC_VPE_EICSS60	32	0	rw	
GIC_VPE_EICSS61	32	0	rw	
GIC_VPE_EICSS62	32	0	rw	
GIC_VPE_EICSS63	32	0	rw	
GIC_Vx_DINT_PART	32	1	rw	
GIC_Cx_BRK_GROUP	32	0	rw	
GIC_VPE_CTL	32	2	rw	

GIC_VPE_PEND	32	0	r-	
GIC_VPE_MASK	32	7f	r-	
GIC_VPE_RMASK	32	0	-w	
GIC_VPE_SMASK	32	0	-w	
GIC_VPE_WD_MAP	32	40000000	rw	
GIC_VPE_COMPARE_MAP	32	80000000	rw	
GIC_VPE_TIMER_MAP	32	80000005	rw	
GIC_VPE_FDC_MAP	32	80000005	rw	
GIC_VPE_PERFCTR_MAP	32	80000005	rw	
GIC_VPE_SWInt0_MAP	32	80000000	rw	
GIC_VPE_SWInt1_MAP	32	80000000	rw	
GIC_VPE_OTHER_ADDRESS	32	0	rw	
GIC_VPE_IDENT	32	0	r-	
GIC_VPE_WD_CONFIG	32	0	rw	
GIC_VPE_WD_COUNT	32	0	r-	
GIC_VPE_WD_INITIAL	32	0	rw	
GIC_VPE_CompareLo	32	ffffffff	rw	
GIC_VPE_CompareHi	32	ffffffff	rw	
GIC_VPE_EICSS00	32	0	rw	
GIC_VPE_EICSS01	32	0	rw	
GIC_VPE_EICSS02	32	0	rw	
GIC_VPE_EICSS03	32	0	rw	
GIC_VPE_EICSS04	32	0	rw	
GIC_VPE_EICSS05	32	0	rw	
GIC_VPE_EICSS06	32	0	rw	
GIC_VPE_EICSS07	32	0	rw	
GIC_VPE_EICSS08	32	0	rw	
GIC_VPE_EICSS09	32	0	rw	
GIC_VPE_EICSS10	32	0	rw	
GIC_VPE_EICSS11	32	0	rw	
GIC_VPE_EICSS12	32	0	rw	
GIC_VPE_EICSS13	32	0	rw	
GIC_VPE_EICSS14	32	0	rw	
GIC_VPE_EICSS15	32	0	rw	
GIC_VPE_EICSS16	32	0	rw	
GIC_VPE_EICSS17	32	0	rw	
GIC_VPE_EICSS18	32	0	rw	
GIC_VPE_EICSS19	32	0	rw	
GIC_VPE_EICSS20	32	0	rw	
GIC_VPE_EICSS21	32	0	rw	
GIC_VPE_EICSS22	32	0	rw	
GIC_VPE_EICSS23	32	0	rw	

GIC_VPE_EICSS24	32	0	rw	
GIC_VPE_EICSS25	32	0	rw	
GIC_VPE_EICSS26	32	0	rw	
GIC_VPE_EICSS27	32	0	rw	
GIC_VPE_EICSS28	32	0	rw	
GIC_VPE_EICSS29	32	0	rw	
GIC_VPE_EICSS30	32	0	rw	
GIC_VPE_EICSS31	32	0	rw	
GIC_VPE_EICSS32	32	0	rw	
GIC_VPE_EICSS33	32	0	rw	
GIC_VPE_EICSS34	32	0	rw	
GIC_VPE_EICSS35	32	0	rw	
GIC_VPE_EICSS36	32	0	rw	
GIC_VPE_EICSS37	32	0	rw	
GIC_VPE_EICSS38	32	0	rw	
GIC_VPE_EICSS39	32	0	rw	
GIC_VPE_EICSS40	32	0	rw	
GIC_VPE_EICSS41	32	0	rw	
GIC_VPE_EICSS42	32	0	rw	
GIC_VPE_EICSS43	32	0	rw	
GIC_VPE_EICSS44	32	0	rw	
GIC_VPE_EICSS45	32	0	rw	
GIC_VPE_EICSS46	32	0	rw	
GIC_VPE_EICSS47	32	0	rw	
GIC_VPE_EICSS48	32	0	rw	
GIC_VPE_EICSS49	32	0	rw	
GIC_VPE_EICSS50	32	0	rw	
GIC_VPE_EICSS51	32	0	rw	
GIC_VPE_EICSS52	32	0	rw	
GIC_VPE_EICSS53	32	0	rw	
GIC_VPE_EICSS54	32	0	rw	
GIC_VPE_EICSS55	32	0	rw	
GIC_VPE_EICSS56	32	0	rw	
GIC_VPE_EICSS57	32	0	rw	
GIC_VPE_EICSS58	32	0	rw	
GIC_VPE_EICSS59	32	0	rw	
GIC_VPE_EICSS60	32	0	rw	
GIC_VPE_EICSS61	32	0	rw	
GIC_VPE_EICSS62	32	0	rw	
GIC_VPE_EICSS63	32	0	rw	
GIC_Vx_DINT_PART	32	1	rw	
GIC_Cx_BRK_GROUP	32	0	rw	

GIC_CounterLoUser	32	0	r-	
GIC_CounterHiUser	32	0	r-	

12.2.10 Integration_support

Table 33. Registers at level 2, type: CPU, register group: 'Integration_support'

Name	Bits	Initial value (Hex)		Description
stop	32	0	rw	write with non-zero to stop processor

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