OVP Guide to Using Processor Models

Model specific information for powerpc_m470

Imperas Software Limited
Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com

Author	Imperas Software Limited
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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

PPC32 Family Processor Model. Providing PPC 400 family variants.

1.2 Licensing

Open Source Apache 2.0

1.3 Limitations

This model is currently under development

The FPU is incomplete

FPU exceptions are not implemented

Some Single Floating Point FPU instructions are not implemented

The MMU is not implemented

1.4 Verification

Basic verification of ISA against golden reference has been performed

1.5 Features

Chapter 2

Configuration

2.1 Location

This model's VLNV is power.ovpworld.org/processor/powerpc32_400/1.0.
The model source is usually at:
$IMPERAS_HOME/ImperasLib/source/power.ovpworld.org/processor/powerpc32_400/1.0
The model binary is usually at:
$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/power.ovpworld.org/processor/powerpc32_400/1.0

2.2 GDB Path

The default GDB for this model is: $IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/powerpc-elf-gdb.

2.3 Semi-Host Library

The default semi-host library file is power.ovpworld.org/semihosting/powerpc32Newlib/1.0

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: 0x14.

Chapter 3

All Variants in this model

This model has these variants

Variant	Description
m476	
m470	(described in this document)
m460	
m440	

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	32	32	mandatory	
DATA	32	32	optional	

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

Name	Type	Description
variant	Enumeration	Selects variant (either a generic UISA or a specific model)
verbose	Boolean	Specify verbose output messages
endian	Endian	Specify Model endian
UISA_I_B	Boolean	UISA Feature UISA_I_B
UISA_I_BCDA	Boolean	UISA Feature UISA_I_BCDA
UISA_I_S	Boolean	UISA Feature UISA_I_S
UISA_I_E	Boolean	UISA Feature UISA_I_E
UISA_I_E_PC	Boolean	UISA Feature UISA_I_E_PC
UISA_I_E_PD	Boolean	UISA Feature UISA_I_E_PD
UISA_I_EC	Boolean	UISA Feature UISA_I_EC
UISA_I_FP	Boolean	UISA Feature UISA_I_FP
UISA_I_DFP	Boolean	UISA Feature UISA_I_DFP
UISA_I_MA	Boolean	UISA Feature UISA_I_MA
UISA_I_SP	Boolean	UISA Feature UISA_I_SP
UISA_I_V	Boolean	UISA Feature UISA_I_V
UISA_I_LMA	Boolean	UISA Feature UISA_I_LMA
UISA_I_WT	Boolean	UISA Feature UISA_I_WT
UISA_I_VLE	Boolean	UISA Feature UISA_I_VLE
ENABLE_FPU	Uns32	Enable FPU At Startup
UNIMP_TO_NOP	Boolean	Map Unimplemented Instructions to NOP
WARN_NOP	Boolean	Warn when executing nop-mapped instructions

Table 8.1: Parameters

Chapter 9

Execution Modes

This model does not have different execution modes.

Chapter 10

Exceptions

Exception	Code
Reset	0
Undefined	1
Arith	2
RdAlign	3
WrAlign	4
RdAbort	5
WrAbort	6
RdPriv	7
WrPriv	8
Fetch	9

Table 10.1: Exceptions implemented by this processor

Chapter 11

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.
OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.
This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1

This level in the model hierarchy has 2 commands.
This level in the model hierarchy has 3 register groups:

Group name	Registers
User	32
FloatingPoint	32
System	7

Table 11.1: Register groups

This level in the model hierarchy has no children.

Chapter 12

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1

12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

Chapter 13

Registers

13.1 Level 1

13.1.1 User

Registers at level:1, group:User

Name	Bits	Initial-Hex	RW	Description
GPR0	32	0	rw	
GPR1	32	0	rw	
GPR2	32	0	rw	
GPR3	32	0	rw	
GPR4	32	0	rw	
GPR5	32	0	rw	
GPR6	32	0	rw	
GPR7	32	0	rw	
GPR8	32	0	rw	
GPR9	32	0	rw	
GPR10	32	0	rw	
GPR11	32	0	rw	
GPR12	32	0	rw	
GPR13	32	0	rw	
GPR14	32	0	rw	
GPR15	32	0	rw	
GPR16	32	0	rw	
GPR17	32	0	rw	
GPR18	32	0	rw	
GPR19	32	0	rw	
GPR20	32	0	rw	
GPR21	32	0	rw	
GPR22	32	0	rw	
GPR23	32	0	rw	
GPR24	32	0	rw	
GPR25	32	0	rw	
GPR26	32	0	rw	
GPR27	32	0	rw	
GPR28	32	0	rw	
GPR29	32	0	rw	
GPR30	32	0	rw	
GPR31	32	0	rw	

Table 13.1: Registers at level 1, group:User

13.1.2 FloatingPoint

Registers at level:1, group:FloatingPoint

Name	Bits	Initial-Hex	RW	Description
FPR0	64	0	rw	
FPR1	64	0	rw	
FPR2	64	0	rw	
FPR3	64	0	rw	
FPR4	64	0	rw	
FPR5	64	0	rw	
FPR6	64	0	rw	
FPR7	64	0	rw	
FPR8	64	0	rw	
FPR9	64	0	rw	
FPR10	64	0	rw	
FPR11	64	0	rw	
FPR12	64	0	rw	
FPR13	64	0	rw	
FPR14	64	0	rw	
FPR15	64	0	rw	
FPR16	64	0	rw	
FPR17	64	0	rw	
FPR18	64	0	rw	
FPR19	64	0	rw	
FPR20	64	0	rw	
FPR21	64	0	rw	
FPR22	64	0	rw	
FPR23	64	0	rw	
FPR24	64	0	rw	
FPR25	64	0	rw	
FPR26	64	0	rw	
FPR27	64	0	rw	
FPR28	64	0	rw	
FPR29	64	0	rw	
FPR30	64	0	rw	
FPR31	64	0	rw	

Table 13.2: Registers at level 1, group:FloatingPoint

13.1.3 System

Registers at level:1, group:System

Name	Bits	Initial-Hex	RW	Description
PC	32	0	rw	program counter
MSR	32	0	rw	
CR	32	0	rw	
LR	32	0	rw	
CTR	32	0	rw	
XER	32	0	rw	
FPSCR	32	0	rw	

Table 13.3: Registers at level 1, group:System