



OVP Guide to Using Processor Models

Model specific information for riscv_RV32EC

Imperas Software Limited
Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com



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Model Release Status

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Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

RISC-V RV32EC 32-bit processor model

1.2 Licensing

This Model is released under the Open Source Apache 2.0

1.3 Features

The model supports the following architectural features, defined in the misa CSR:

extension C (compressed instructions)

RV32E base ISA

extension S (Supervisor mode)

extension U (User mode)

32-bit XLEN

If required, supported architectural features may be overridden using parameter “`misa_Extensions`”. Parameter “`misa_Extensions_mask`” can be used to specify which features can be dynamically enabled or disabled by writes to the `misa` register.

On this variant, the Machine trap-vector base-address register (`mtvec`) is writable. It can instead be configured as read-only using parameter “`mtvec_is_ro`”.

Values written to “`mtvec`” are masked using the value `0xfffffd`. A different mask of writable bits may be specified using parameter “`mtvec_mask`” if required. In addition, when Vectored interrupt mode is enabled, parameter “`tvec_align`” may be used to specify additional hardware-enforced base address alignment. In this variant, “`tvec_align`” defaults to 0, implying no alignment constraint.

The initial value of “`mtvec`” is `0x0`. A different value may be specified using parameter “`mtvec`” if required.

Values written to “`stvec`” are masked using the value `0xfffffd`. A different mask of writable bits may be specified using parameter “`stvec_mask`” if required. parameter “`tvec_align`” may be used to specify additional hardware-enforced base address alignment in the same manner as for the “`mtvec`” register, described above.

On reset, the model will restart at address `0x0`. A different reset address may be specified using parameter “`reset_address`” if required.

On an NMI, the model will restart at address `0x0`. A different NMI address may be specified using parameter “`nmi_address`” if required.

WFI will halt the processor until an interrupt occurs. It can instead be configured as a NOP using parameter “`wfi_is_nop`”. WFI timeout wait is implemented with a time limit of 0 (i.e. WFI causes an Illegal Instruction trap in Supervisor mode when `mstatus.TW=1`).

The “`cycle`” CSR is implemented in this variant. Set parameter “`cycle_undefined`” to True to instead specify that “`cycle`” is unimplemented and reads of it should trap to Machine mode.

The “`time`” CSR is implemented in this variant. Set parameter “`time_undefined`” to True to instead specify that “`time`” is unimplemented and reads of it should trap to Machine mode. Usually, the value of the “`time`” CSR should be provided by the platform - see notes below about the artifact “`CSR`” bus for information about how this is done.

The “`instret`” CSR is implemented in this variant. Set parameter “`instret_undefined`” to True to instead specify that “`instret`” is unimplemented and reads of it should trap to Machine mode.

A 9-bit ASID is implemented. Use parameter “`ASID_bits`” to specify a different implemented ASID size if required.

This variant supports address translation modes 0 and 1. Use parameter “`Sv_modes`” to specify a bit mask of different modes if required.

Unaligned memory accesses are not supported by this variant. Set parameter “`unaligned`” to “`T`”

to enable such accesses.

16 PMP entries are implemented by this variant. Use parameter “PMP_registers” to specify a different number of PMP entries; set the parameter to 0 to disable the PMP unit.

1.4 Interrupts

The “reset” port is an active-high reset input. The processor is halted when “reset” goes high and resumes execution from the reset address specified using the “reset_address” parameter when the signal goes low. The “mcause” register is cleared to zero.

The “nmi” port is an active-high NMI input. The processor is halted when “nmi” goes high and resumes execution from the address specified using the “nmi_address” parameter when the signal goes low. The “mcause” register is cleared to zero.

All other interrupt ports are active high.

1.5 Debug Mask

It is possible to enable model debug messages in various categories. This can be done statically using the “override_debugMask” parameter, or dynamically using the “debugflags” command. Enabled messages are specified using a bitmask value, as follows:

Value 0x002: enable debugging of PMP and virtual memory state;

Value 0x004: enable debugging of interrupt state.

All other bits in the debug bitmask are reserved and must not be set to non-zero values.

1.6 Integration Support

This model implements a number of non-architectural pseudo-registers and other features to facilitate integration.

1.6.1 CSR Register External Implementation

If parameter “enable_CSR_bus” is True, an artifact 16-bit bus “CSR” is enabled. Slave callbacks installed on this bus can be used to implement modified CSR behavior (use opBusSlaveNew or icmMapExternalMemory, depending on the client API). A CSR with index 0xABC is mapped on the bus at address 0xABC0; as a concrete example, implementing CSR “time” (number 0xC01) externally requires installation of callbacks at address 0xC010 on the CSR bus.

1.7 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. fence.i) are treated as NOPs, with the exception of any Illegal Instruction behavior, which is modeled.

Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous. Data barrier instructions (e.g. fence) are treated as NOPs, with the exception of any Illegal Instruction behavior, which is modeled.

Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.

Hardware Performance Monitor and Debug registers are not implemented and hardwired to zero.

The TLB is architecturally-accurate but not device accurate. This means that all TLB maintenance and address translation operations are fully implemented but the cache is larger than in the real device.

1.8 Verification

All instructions have been extensively tested by Imperas, using tests generated specifically for this model and also reference tests from <https://github.com/riscv/riscv-tests>.

1.9 References

The Model details are based upon the following specifications:

- RISC-V Instruction Set Manual, Volume I: User-Level ISA (User Architecture Version 2.2)
- RISC-V Instruction Set Manual, Volume II: Privileged Architecture (Privileged Architecture Version 1.10)

Chapter 2

Configuration

2.1 Location

This model's VLN is `riscv.ovpworld.org/processor/riscv/1.0`.

The model source is usually at:

`$IMPERAS_HOME/ImperasLib/source/riscv.ovpworld.org/processor/riscv/1.0`

The model binary is usually at:

`$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/riscv.ovpworld.org/processor/riscv/1.0`

2.2 GDB Path

The default GDB for this model is: `$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/riscv64-unknown-elf-gdb`.

2.3 Semi-Host Library

The default semi-host library file is `riscv.ovpworld.org/semihosting/riscv32Newlib/1.0`

2.4 Processor Endian-ness

This is a LITTLE endian model.

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: `0xf3`.

Chapter 3

All Variants in this model

This model has these variants

Variant	Description
RV32I	
RV32IM	
RV32IMC	
RV32IMAC	
RV32G	
RV32GC	
RV32GCN	
RV32E	
RV32EC	(described in this document)
RV64I	
RV64IM	
RV64IMC	
RV64IMAC	
RV64G	
RV64GC	
RV64GCN	

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

Name	min	max	Connect?	Description
INSTRUCTION	32	34	mandatory	Instruction bus
DATA	32	34	optional	Data bus

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

Name	Type	Connect?	Description
reset	input	optional	Reset
nmi	input	optional	NMI
SSWInterrupt	input	optional	Supervisor software interrupt
MSWInterrupt	input	optional	Machine software interrupt
STimerInterrupt	input	optional	Supervisor timer interrupt
MTimerInterrupt	input	optional	Machine timer interrupt
SExternalInterrupt	input	optional	Supervisor external interrupt
MExternalInterrupt	input	optional	Machine external interrupt

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

Name	Type	Description
variant	Enumeration	Selects variant (either a generic UISA or a specific model)
user_version	Enumeration	Specify required User Architecture version(2.2 or 2.3)
priv_version	Enumeration	Specify required Privileged Architecture version(1.10 or 1.11)
verbose	Boolean	Specify verbose output messages
updatePTEA	Boolean	Specify whether hardware update of PTE A bit is supported
updatePTED	Boolean	Specify whether hardware update of PTE D bit is supported
unaligned	Boolean	Specify whether the processor supports unaligned memory accesses
wfi_is_nop	Boolean	Specify whether WFI should be treated as a NOP (if not, halt while waiting for interrupts)
mtvec_is_ro	Boolean	Specify whether mtvec CSR is read-only
tvec_align	Uns32	Specify hardware-enforced alignment of mtvec/stvec/utvec when Vectored interrupt mode enabled
mtvec_mask	Uns64	Specify hardware-enforced mask of writable bits in mtvec register
stvec_mask	Uns64	Specify hardware-enforced mask of writable bits in stvec register
tval_ii_code	Boolean	Specify whether mtval/stval contain faulting instruction bits on illegal instruction exception
cycle_undefined	Boolean	Specify that the cycle CSR is undefined (reads to it are emulated by a Machine mode trap)
time_undefined	Boolean	Specify that the time CSR is undefined (reads to it are emulated by a Machine mode trap)
instret_undefined	Boolean	Specify that the instret CSR is undefined (reads to it are emulated by a Machine mode trap)
enable_CSR_bus	Boolean	Add artifact CSR bus port, allowing CSR registers to be externally implemented
ASID_bits	Uns32	Specify the number of implemented ASID bits
reset_address	Uns64	Override reset vector address
nmi_address	Uns64	Override NMI vector address
PMP_registers	Uns32	Specify the number of implemented PMP address registers
Sv_modes	Uns32	Specify bit mask of implemented Sv modes (e.g. $1 \ll 8$ is Sv39)
local_int_num	Uns32	Specify number of supplemental local interrupts
endian	Endian	Model endian
misa_MXL	Uns32	Override default value of misa.MXL
misa_MXL_mask	Uns32	Override mask of writable bits in misa.MXL
misa_Extensions	Uns32	Override default value of misa.Extensions
misa_Extensions_mask	Uns32	Override mask of writable bits in misa.Extensions
mvendorid	Uns64	Override mvendorid register
marchid	Uns64	Override marchid register
mimpid	Uns64	Override mimpid register
mhartid	Uns64	Override mhartid register
mtvec	Uns64	Override mtvec register

Table 8.1: Parameters that can be set in: Hart

8.1 Parameters with enumerated types

8.1.1 Parameter user_version

Set to this value	Description
2.2	User Architecture Version 2.2
2.3	User Architecture Version 2.3-draft

Table 8.2: Values for Parameter user_version

8.1.2 Parameter priv_version

Set to this value	Description
1.10	Privileged Architecture Version 1.10
1.11	Privileged Architecture Version 1.11-draft

Table 8.3: Values for Parameter priv_version

Chapter 9

Execution Modes

Mode	Code	Description
User	0	User mode
Supervisor	1	Supervisor mode
Machine	3	Machine mode

Table 9.1: Modes implemented in: Hart

Chapter 10

Exceptions

Exception	Code	Description
InstructionAddressMisaligned	0	Fetch from unaligned address
InstructionAccessFault	1	No access permission for fetch
IllegalInstruction	2	Undecoded, unimplemented or disabled instruction
Breakpoint	3	EBREAK instruction executed
LoadAddressMisaligned	4	Load from unaligned address
LoadAccessFault	5	No access permission for load
StoreAMOAddressMisaligned	6	Store/atomic memory operation at unaligned address
StoreAMOAccessFault	7	No access permission for store/atomic memory operation
EnvironmentCallFromUMode	8	ECALL instruction executed in User mode
EnvironmentCallFromSMode	9	ECALL instruction executed in Supervisor mode
EnvironmentCallFromMMode	11	ECALL instruction executed in Machine mode
InstructionPageFault	12	Page fault at fetch address
LoadPageFault	13	Page fault at load address
StoreAMOPageFault	15	Page fault at store/atomic memory operation address
SSWInterrupt	65	Supervisor software interrupt
MSWInterrupt	67	Machine software interrupt
STimerInterrupt	69	Supervisor timer interrupt
MTimerInterrupt	71	Machine timer interrupt
SExternalInterrupt	73	Supervisor external interrupt
MExternalInterrupt	75	Machine external interrupt

Table 10.1: Exceptions implemented in: Hart

Chapter 11

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1: Hart

This level in the model hierarchy has 3 commands.

This level in the model hierarchy has 4 register groups:

Group name	Registers
Core	17
User_Control_and_Status	64
Supervisor_Control_and_Status	10
Machine_Control_and_Status	134

Table 11.1: Register groups

This level in the model hierarchy has no children.

Chapter 12

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1: Hart

12.1.1 dumpTLB

12.1.1.1 Argument description

show TLB contents

12.1.2 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

12.1.3 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments

Chapter 13

Registers

13.1 Level 1: Hart

13.1.1 Core

Registers at level:1, type:Hart group:Core

Name	Bits	Initial-Hex	RW	Description
zero	32	0	r-	
ra	32	0	rw	
sp	32	0	rw	stack pointer
gp	32	0	rw	
tp	32	0	rw	
t0	32	0	rw	
t1	32	0	rw	
t2	32	0	rw	
s0	32	0	rw	
s1	32	0	rw	
a0	32	0	rw	
a1	32	0	rw	
a2	32	0	rw	
a3	32	0	rw	
a4	32	0	rw	
a5	32	0	rw	
pc	32	0	rw	program counter

Table 13.1: Registers at level 1, type:Hart group:Core

13.1.2 User_Control_and_Status

Registers at level:1, type:Hart group:User_Control_and_Status

Name	Bits	Initial-Hex	RW	Description
cycle	32	0	r-	Cycle Counter
time	32	0	r-	Timer
instret	32	0	r-	Instructions Retired
hpmcounter3	32	-	r-	Performance Monitor Counter 3 (hardwired to zero)
hpmcounter4	32	-	r-	Performance Monitor Counter 4 (hardwired to zero)
hpmcounter5	32	-	r-	Performance Monitor Counter 5 (hardwired to zero)
hpmcounter6	32	-	r-	Performance Monitor Counter 6 (hardwired to zero)
hpmcounter7	32	-	r-	Performance Monitor Counter 7 (hardwired to zero)

hpmcounter8	32	-	r-	Performance Monitor Counter 8 (hardwired to zero)
hpmcounter9	32	-	r-	Performance Monitor Counter 9 (hardwired to zero)
hpmcounter10	32	-	r-	Performance Monitor Counter 10 (hardwired to zero)
hpmcounter11	32	-	r-	Performance Monitor Counter 11 (hardwired to zero)
hpmcounter12	32	-	r-	Performance Monitor Counter 12 (hardwired to zero)
hpmcounter13	32	-	r-	Performance Monitor Counter 13 (hardwired to zero)
hpmcounter14	32	-	r-	Performance Monitor Counter 14 (hardwired to zero)
hpmcounter15	32	-	r-	Performance Monitor Counter 15 (hardwired to zero)
hpmcounter16	32	-	r-	Performance Monitor Counter 16 (hardwired to zero)
hpmcounter17	32	-	r-	Performance Monitor Counter 17 (hardwired to zero)
hpmcounter18	32	-	r-	Performance Monitor Counter 18 (hardwired to zero)
hpmcounter19	32	-	r-	Performance Monitor Counter 19 (hardwired to zero)
hpmcounter20	32	-	r-	Performance Monitor Counter 20 (hardwired to zero)
hpmcounter21	32	-	r-	Performance Monitor Counter 21 (hardwired to zero)
hpmcounter22	32	-	r-	Performance Monitor Counter 22 (hardwired to zero)
hpmcounter23	32	-	r-	Performance Monitor Counter 23 (hardwired to zero)
hpmcounter24	32	-	r-	Performance Monitor Counter 24 (hardwired to zero)
hpmcounter25	32	-	r-	Performance Monitor Counter 25 (hardwired to zero)
hpmcounter26	32	-	r-	Performance Monitor Counter 26 (hardwired to zero)
hpmcounter27	32	-	r-	Performance Monitor Counter 27 (hardwired to zero)
hpmcounter28	32	-	r-	Performance Monitor Counter 28 (hardwired to zero)
hpmcounter29	32	-	r-	Performance Monitor Counter 29 (hardwired to zero)
hpmcounter30	32	-	r-	Performance Monitor Counter 30 (hardwired to zero)
hpmcounter31	32	-	r-	Performance Monitor Counter 31 (hardwired to zero)
cycleh	32	0	r-	Cycle Counter High
timeh	32	0	r-	Timer High
instreth	32	0	r-	Instructions Retired High
hpmcounterh3	32	-	r-	Performance Monitor High 3 (hardwired to zero)
hpmcounterh4	32	-	r-	Performance Monitor High 4 (hardwired to zero)
hpmcounterh5	32	-	r-	Performance Monitor High 5 (hardwired to zero)
hpmcounterh6	32	-	r-	Performance Monitor High 6 (hardwired to zero)
hpmcounterh7	32	-	r-	Performance Monitor High 7 (hardwired to zero)
hpmcounterh8	32	-	r-	Performance Monitor High 8 (hardwired to zero)
hpmcounterh9	32	-	r-	Performance Monitor High 9 (hardwired to zero)
hpmcounterh10	32	-	r-	Performance Monitor High 10 (hardwired to zero)
hpmcounterh11	32	-	r-	Performance Monitor High 11 (hardwired to zero)
hpmcounterh12	32	-	r-	Performance Monitor High 12 (hardwired to zero)
hpmcounterh13	32	-	r-	Performance Monitor High 13 (hardwired to zero)
hpmcounterh14	32	-	r-	Performance Monitor High 14 (hardwired to zero)
hpmcounterh15	32	-	r-	Performance Monitor High 15 (hardwired to zero)
hpmcounterh16	32	-	r-	Performance Monitor High 16 (hardwired to zero)
hpmcounterh17	32	-	r-	Performance Monitor High 17 (hardwired to zero)
hpmcounterh18	32	-	r-	Performance Monitor High 18 (hardwired to zero)
hpmcounterh19	32	-	r-	Performance Monitor High 19 (hardwired to zero)
hpmcounterh20	32	-	r-	Performance Monitor High 20 (hardwired to zero)
hpmcounterh21	32	-	r-	Performance Monitor High 21 (hardwired to zero)
hpmcounterh22	32	-	r-	Performance Monitor High 22 (hardwired to zero)
hpmcounterh23	32	-	r-	Performance Monitor High 23 (hardwired to zero)
hpmcounterh24	32	-	r-	Performance Monitor High 24 (hardwired to zero)
hpmcounterh25	32	-	r-	Performance Monitor High 25 (hardwired to zero)
hpmcounterh26	32	-	r-	Performance Monitor High 26 (hardwired to zero)
hpmcounterh27	32	-	r-	Performance Monitor High 27 (hardwired to zero)
hpmcounterh28	32	-	r-	Performance Monitor High 28 (hardwired to zero)
hpmcounterh29	32	-	r-	Performance Monitor High 29 (hardwired to zero)
hpmcounterh30	32	-	r-	Performance Monitor High 30 (hardwired to zero)
hpmcounterh31	32	-	r-	Performance Monitor High 31 (hardwired to zero)

Table 13.2: Registers at level 1, type:Hart group:User_Control_and_Status

13.1.3 Supervisor_Control_and_Status

Registers at level:1, type:Hart group:Supervisor_Control_and_Status

Name	Bits	Initial-Hex	RW	Description
sstatus	32	0	rw	Supervisor Status
sie	32	0	rw	Supervisor Interrupt Enable
stvec	32	0	rw	Supervisor Trap-Vector Base-Address
scounteren	32	0	rw	Supervisor Counter Enable
sscratch	32	0	rw	Supervisor Scratch
sepc	32	0	rw	Supervisor Exception Program Counter
scause	32	0	rw	Supervisor Cause
stval	32	0	rw	Supervisor Trap Value
sip	32	0	rw	Supervisor Interrupt Pending
satp	32	0	rw	Supervisor Address Translation and Protection

Table 13.3: Registers at level 1, type:Hart group:Supervisor_Control_and_Status

13.1.4 Machine_Control_and_Status

Registers at level:1, type:Hart group:Machine_Control_and_Status

Name	Bits	Initial-Hex	RW	Description
mstatus	32	0	rw	Machine Status
misa	32	40140014	rw	ISA and Extensions
medeleg	32	0	rw	Machine Exception Delegation
mideleg	32	0	rw	Machine Interrupt Delegation
mie	32	0	rw	Machine Interrupt Enable
mtvec	32	0	rw	Machine Trap-Vector Base-Address
mcounteren	32	0	rw	Machine Counter Enable
mhpmevent3	32	-	rw	Machine Performance Monitor Event Select 3 (hardwired to zero)
mhpmevent4	32	-	rw	Machine Performance Monitor Event Select 4 (hardwired to zero)
mhpmevent5	32	-	rw	Machine Performance Monitor Event Select 5 (hardwired to zero)
mhpmevent6	32	-	rw	Machine Performance Monitor Event Select 6 (hardwired to zero)
mhpmevent7	32	-	rw	Machine Performance Monitor Event Select 7 (hardwired to zero)
mhpmevent8	32	-	rw	Machine Performance Monitor Event Select 8 (hardwired to zero)
mhpmevent9	32	-	rw	Machine Performance Monitor Event Select 9 (hardwired to zero)
mhpmevent10	32	-	rw	Machine Performance Monitor Event Select 10 (hardwired to zero)
mhpmevent11	32	-	rw	Machine Performance Monitor Event Select 11 (hardwired to zero)
mhpmevent12	32	-	rw	Machine Performance Monitor Event Select 12 (hardwired to zero)
mhpmevent13	32	-	rw	Machine Performance Monitor Event Select 13 (hardwired to zero)
mhpmevent14	32	-	rw	Machine Performance Monitor Event Select 14 (hardwired to zero)
mhpmevent15	32	-	rw	Machine Performance Monitor Event Select 15 (hardwired to zero)
mhpmevent16	32	-	rw	Machine Performance Monitor Event Select 16 (hardwired to zero)
mhpmevent17	32	-	rw	Machine Performance Monitor Event Select 17 (hardwired to zero)
mhpmevent18	32	-	rw	Machine Performance Monitor Event Select 18 (hardwired to zero)
mhpmevent19	32	-	rw	Machine Performance Monitor Event Select 19 (hardwired to zero)
mhpmevent20	32	-	rw	Machine Performance Monitor Event Select 20 (hardwired to zero)
mhpmevent21	32	-	rw	Machine Performance Monitor Event Select 21 (hardwired to zero)
mhpmevent22	32	-	rw	Machine Performance Monitor Event Select 22 (hardwired to zero)
mhpmevent23	32	-	rw	Machine Performance Monitor Event Select 23 (hardwired to zero)
mhpmevent24	32	-	rw	Machine Performance Monitor Event Select 24 (hardwired to zero)

mhpmevent25	32	-	rw	Machine Performance Monitor Event Select 25 (hardwired to zero)
mhpmevent26	32	-	rw	Machine Performance Monitor Event Select 26 (hardwired to zero)
mhpmevent27	32	-	rw	Machine Performance Monitor Event Select 27 (hardwired to zero)
mhpmevent28	32	-	rw	Machine Performance Monitor Event Select 28 (hardwired to zero)
mhpmevent29	32	-	rw	Machine Performance Monitor Event Select 29 (hardwired to zero)
mhpmevent30	32	-	rw	Machine Performance Monitor Event Select 30 (hardwired to zero)
mhpmevent31	32	-	rw	Machine Performance Monitor Event Select 31 (hardwired to zero)
mscratch	32	0	rw	Machine Scratch
mepc	32	0	rw	Machine Exception Program Counter
mcause	32	0	rw	Machine Cause
mtval	32	0	rw	Machine Trap Value
mip	32	0	rw	Machine Interrupt Pending
pmpcfg0	32	0	rw	Physical Memory Protection Configuration 0
pmpcfg1	32	0	rw	Physical Memory Protection Configuration 1
pmpcfg2	32	0	rw	Physical Memory Protection Configuration 2
pmpcfg3	32	0	rw	Physical Memory Protection Configuration 3
pmpaddr0	32	0	rw	Physical Memory Protection Address 0
pmpaddr1	32	0	rw	Physical Memory Protection Address 1
pmpaddr2	32	0	rw	Physical Memory Protection Address 2
pmpaddr3	32	0	rw	Physical Memory Protection Address 3
pmpaddr4	32	0	rw	Physical Memory Protection Address 4
pmpaddr5	32	0	rw	Physical Memory Protection Address 5
pmpaddr6	32	0	rw	Physical Memory Protection Address 6
pmpaddr7	32	0	rw	Physical Memory Protection Address 7
pmpaddr8	32	0	rw	Physical Memory Protection Address 8
pmpaddr9	32	0	rw	Physical Memory Protection Address 9
pmpaddr10	32	0	rw	Physical Memory Protection Address 10
pmpaddr11	32	0	rw	Physical Memory Protection Address 11
pmpaddr12	32	0	rw	Physical Memory Protection Address 12
pmpaddr13	32	0	rw	Physical Memory Protection Address 13
pmpaddr14	32	0	rw	Physical Memory Protection Address 14
pmpaddr15	32	0	rw	Physical Memory Protection Address 15
tselect	32	-	rw	Debug/Trace Trigger Register Select (not implemented)
tdata1	32	-	rw	Debug/Trace Trigger Data 1 (not implemented)
tdata2	32	-	rw	Debug/Trace Trigger Data 2 (not implemented)
tdata3	32	-	rw	Debug/Trace Trigger Data 3 (not implemented)
dcsr	32	-	rw	Debug Control and Status (not implemented)
dpc	32	-	rw	Debug PC (not implemented)
dscratch	32	-	rw	Debug Scratch (not implemented)
mcycle	32	0	rw	Machine Cycle Counter
minstret	32	0	rw	Machine Instructions Retired
mhpcounter3	32	-	rw	Machine Performance Monitor Counter 3 (hardwired to zero)
mhpcounter4	32	-	rw	Machine Performance Monitor Counter 4 (hardwired to zero)
mhpcounter5	32	-	rw	Machine Performance Monitor Counter 5 (hardwired to zero)
mhpcounter6	32	-	rw	Machine Performance Monitor Counter 6 (hardwired to zero)
mhpcounter7	32	-	rw	Machine Performance Monitor Counter 7 (hardwired to zero)
mhpcounter8	32	-	rw	Machine Performance Monitor Counter 8 (hardwired to zero)
mhpcounter9	32	-	rw	Machine Performance Monitor Counter 9 (hardwired to zero)
mhpcounter10	32	-	rw	Machine Performance Monitor Counter 10 (hardwired to zero)
mhpcounter11	32	-	rw	Machine Performance Monitor Counter 11 (hardwired to zero)
mhpcounter12	32	-	rw	Machine Performance Monitor Counter 12 (hardwired to zero)
mhpcounter13	32	-	rw	Machine Performance Monitor Counter 13 (hardwired to zero)
mhpcounter14	32	-	rw	Machine Performance Monitor Counter 14 (hardwired to zero)
mhpcounter15	32	-	rw	Machine Performance Monitor Counter 15 (hardwired to zero)
mhpcounter16	32	-	rw	Machine Performance Monitor Counter 16 (hardwired to zero)
mhpcounter17	32	-	rw	Machine Performance Monitor Counter 17 (hardwired to zero)

mhpmcounter18	32	-	rw	Machine Performance Monitor Counter 18 (hardwired to zero)
mhpmcounter19	32	-	rw	Machine Performance Monitor Counter 19 (hardwired to zero)
mhpmcounter20	32	-	rw	Machine Performance Monitor Counter 20 (hardwired to zero)
mhpmcounter21	32	-	rw	Machine Performance Monitor Counter 21 (hardwired to zero)
mhpmcounter22	32	-	rw	Machine Performance Monitor Counter 22 (hardwired to zero)
mhpmcounter23	32	-	rw	Machine Performance Monitor Counter 23 (hardwired to zero)
mhpmcounter24	32	-	rw	Machine Performance Monitor Counter 24 (hardwired to zero)
mhpmcounter25	32	-	rw	Machine Performance Monitor Counter 25 (hardwired to zero)
mhpmcounter26	32	-	rw	Machine Performance Monitor Counter 26 (hardwired to zero)
mhpmcounter27	32	-	rw	Machine Performance Monitor Counter 27 (hardwired to zero)
mhpmcounter28	32	-	rw	Machine Performance Monitor Counter 28 (hardwired to zero)
mhpmcounter29	32	-	rw	Machine Performance Monitor Counter 29 (hardwired to zero)
mhpmcounter30	32	-	rw	Machine Performance Monitor Counter 30 (hardwired to zero)
mhpmcounter31	32	-	rw	Machine Performance Monitor Counter 31 (hardwired to zero)
mcycleh	32	0	rw	Machine Cycle Counter High
minstreth	32	0	rw	Machine Instructions Retired High
mhpmcounterh3	32	-	rw	Machine Performance Monitor Counter High 3 (hardwired to zero)
mhpmcounterh4	32	-	rw	Machine Performance Monitor Counter High 4 (hardwired to zero)
mhpmcounterh5	32	-	rw	Machine Performance Monitor Counter High 5 (hardwired to zero)
mhpmcounterh6	32	-	rw	Machine Performance Monitor Counter High 6 (hardwired to zero)
mhpmcounterh7	32	-	rw	Machine Performance Monitor Counter High 7 (hardwired to zero)
mhpmcounterh8	32	-	rw	Machine Performance Monitor Counter High 8 (hardwired to zero)
mhpmcounterh9	32	-	rw	Machine Performance Monitor Counter High 9 (hardwired to zero)
mhpmcounterh10	32	-	rw	Machine Performance Monitor Counter High 10 (hardwired to zero)
mhpmcounterh11	32	-	rw	Machine Performance Monitor Counter High 11 (hardwired to zero)
mhpmcounterh12	32	-	rw	Machine Performance Monitor Counter High 12 (hardwired to zero)
mhpmcounterh13	32	-	rw	Machine Performance Monitor Counter High 13 (hardwired to zero)
mhpmcounterh14	32	-	rw	Machine Performance Monitor Counter High 14 (hardwired to zero)
mhpmcounterh15	32	-	rw	Machine Performance Monitor Counter High 15 (hardwired to zero)
mhpmcounterh16	32	-	rw	Machine Performance Monitor Counter High 16 (hardwired to zero)
mhpmcounterh17	32	-	rw	Machine Performance Monitor Counter High 17 (hardwired to zero)
mhpmcounterh18	32	-	rw	Machine Performance Monitor Counter High 18 (hardwired to zero)
mhpmcounterh19	32	-	rw	Machine Performance Monitor Counter High 19 (hardwired to zero)
mhpmcounterh20	32	-	rw	Machine Performance Monitor Counter High 20 (hardwired to zero)
mhpmcounterh21	32	-	rw	Machine Performance Monitor Counter High 21 (hardwired to zero)
mhpmcounterh22	32	-	rw	Machine Performance Monitor Counter High 22 (hardwired to zero)
mhpmcounterh23	32	-	rw	Machine Performance Monitor Counter High 23 (hardwired to zero)
mhpmcounterh24	32	-	rw	Machine Performance Monitor Counter High 24 (hardwired to zero)
mhpmcounterh25	32	-	rw	Machine Performance Monitor Counter High 25 (hardwired to zero)
mhpmcounterh26	32	-	rw	Machine Performance Monitor Counter High 26 (hardwired to zero)
mhpmcounterh27	32	-	rw	Machine Performance Monitor Counter High 27 (hardwired to zero)
mhpmcounterh28	32	-	rw	Machine Performance Monitor Counter High 28 (hardwired to zero)
mhpmcounterh29	32	-	rw	Machine Performance Monitor Counter High 29 (hardwired to zero)
mhpmcounterh30	32	-	rw	Machine Performance Monitor Counter High 30 (hardwired to zero)
mhpmcounterh31	32	-	rw	Machine Performance Monitor Counter High 31 (hardwired to zero)
mvendorid	32	0	r-	Vendor ID
marchid	32	0	r-	Architecture ID
mimpid	32	0	r-	Implementation ID
mhartid	32	0	r-	Hardware Thread ID

Table 13.4: Registers at level 1, type:Hart group:Machine_Control_and_Status