



## OVP Guide to Using Processor Models

### Model specific information for SiFive\_S21

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## Model Release Status

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# Chapter 1

## Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

### 1.1 Description

RISC-V S21 64-bit processor model

### 1.2 Licensing

This Model is released under the Open Source Apache 2.0

## 1.3 Extensions

### 1.3.1 Extensions Enabled by Default

The model has the following architectural extensions enabled, and the corresponding bits in the misa CSR Extensions field will be set upon reset:

misa bit 0: extension A (atomic instructions)

misa bit 1: extension B (bit manipulation extension)

misa bit 2: extension C (compressed instructions)

misa bit 8: RV32I/RV64I/RV128I base integer instruction set

misa bit 12: extension M (integer multiply/divide instructions)

misa bit 20: extension U (User mode)

To specify features that can be dynamically enabled or disabled by writes to the misa register in addition to those listed above, use parameter “add\_Extensions\_mask”. This is a string parameter containing the feature letters to add; for example, value “DV” indicates that double-precision floating point and the Vector Extension can be enabled or disabled by writes to the misa register, if supported on this variant. Parameter “sub\_Extensions\_mask” can be used to disable dynamic update of features in the same way.

Legacy parameter “misa\_Extensions\_mask” can also be used. This Uns32-valued parameter specifies all writable bits in the misa Extensions field, replacing any permitted bits defined in the base variant.

Note that any features that are indicated as present in the misa mask but absent in the misa will be ignored. See the next section.

### 1.3.2 Enabling Other Extensions

The following extensions are supported by the model, but not enabled by default in this variant:

misa bit 3: extension D (double-precision floating point)

misa bit 5: extension F (single-precision floating point)

To add features from this list to the visible set in the misa register, use parameter “add\_Extensions”. This is a string containing identification letters of features to enable; for example, value “DV” indicates that double-precision floating point and the Vector Extension should be enabled, if they are currently absent and are available on this variant.

Legacy parameter “misa\_Extensions” can also be used. This Uns32-valued parameter specifies the reset value for the misa CSR Extensions field, replacing any permitted bits defined in the base variant.

To add features from this list to the implicitly-enabled set (not visible in the misa register), use parameter “add\_implicit\_Extensions”. This is a string parameter in the same format as the “add\_Extensions” parameter described above.

### 1.3.3 Disabling Extensions

The following extensions are enabled by default in the model and can be disabled:

misa bit 0: extension A (atomic instructions)

misa bit 1: extension B (bit manipulation extension)

misa bit 12: extension M (integer multiply/divide instructions)

misa bit 20: extension U (User mode)

To disable features that are enabled by default, use parameter “sub\_Extensions”. This is a string containing identification letters of features to disable; for example, value “DF” indicates that double-precision and single-precision floating point extensions should be disabled, if they are enabled by default on this variant.

To remove features from this list from the implicitly-enabled set (not visible in the misa register), use parameter “sub\_implicit\_Extensions”. This is a string parameter in the same format as the “sub\_Extensions” parameter described above.

## 1.4 General Features

### 1.4.1 Multicore Features

This is a multicore variant with 1 harts by default. The number of harts may be overridden with the “numHarts” parameter.

### 1.4.2 mtvec CSR

On this variant, the Machine trap-vector base-address register (mtvec) is writable. It can instead be configured as read-only using parameter “mtvec\_is\_ro”.

Values written to “mtvec” are masked using the value 0x3fffffff. A different mask of writable bits may be specified using parameter “mtvec\_mask” if required. In addition, when Vectored interrupt mode is enabled, parameter “tvec\_align” may be used to specify additional hardware-enforced base address alignment. In this variant, “tvec\_align” defaults to 64.

If parameter “mtvec\_sext” is True, values written to “mtvec” are sign-extended from the most-significant writable bit. In this variant, “mtvec\_sext” is False, indicating that “mtvec” is not sign-extended.

The initial value of “mtvec” is 0x0. A different value may be specified using parameter “mtvec” if required.

### 1.4.3 Reset

On reset, the model will restart at address 0x0. A different reset address may be specified using parameter “reset\_address” or applied using optional input port “reset\_addr” if required.



#### 1.4.4 NMI

On an NMI, the model will restart at address 0x0; a different NMI address may be specified using parameter “nmi\_address” or applied using optional input port “nmi\_addr” if required. The cause reported on an NMI is 0x2 by default; a different cause may be specified using parameter “ecode\_nmi” or applied using optional input port “nmi\_cause” if required.

If parameter “rnmi\_version” is not “none”, resumable NMIs are supported, managed by additional CSRs “mnscratch”, “mnepc”, “mncause” and “mnstatus”, following the indicated version of the Resumable NMI extension proposal. In this variant, “rnmi\_version” is “0.2.1”.

The NMI input is level-sensitive. To instead specify that the NMI input is latched on the rising edge of the NMI signal, set parameter “nmi\_is\_latched” to True.

#### 1.4.5 WFI

WFI will halt the processor until an interrupt occurs. It can instead be configured as a NOP using parameter “wfi\_is\_nop”. WFI timeout wait is implemented with a time limit of 0 (i.e. WFI causes an Illegal Instruction trap in Supervisor mode when mstatus.TW=1).

#### 1.4.6 cycle CSR

The “cycle” CSR is implemented in this variant. Set parameter “cycle\_undefined” to True to instead specify that “cycle” is unimplemented and accesses should cause Illegal Instruction traps.

#### 1.4.7 instret CSR

The “instret” CSR is implemented in this variant. Set parameter “instret\_undefined” to True to instead specify that “instret” is unimplemented and accesses should cause Illegal Instruction traps.

#### 1.4.8 hpmcounter CSR

The “hpmcounter” CSRs are implemented in this variant. Set parameter “hpmcounter\_undefined” to True to instead specify that “hpmcounter” CSRs are unimplemented and accesses should cause Illegal Instruction traps.

#### 1.4.9 time CSR

The “time” CSR is not implemented in this variant and reads of it will cause Illegal Instruction traps. Set parameter “time\_undefined” to False to instead specify that “time” is implemented.

#### 1.4.10 mcycle CSR

The “mcycle” CSR is implemented in this variant. Set parameter “mcycle\_undefined” to True to instead specify that “mcycle” is unimplemented and accesses should cause Illegal Instruction traps.

#### 1.4.11 minstret CSR

The “minstret” CSR is implemented in this variant. Set parameter “minstret\_undefined” to True to instead specify that “minstret” is unimplemented and accesses should cause Illegal Instruction traps.

#### 1.4.12 mhpmcounter CSR

The “mhpmcounter” CSRs are implemented in this variant. Set parameter “mhpmcounter\_undefined” to True to instead specify that “mhpmcounter” CSRs are unimplemented and accesses should cause Illegal Instruction traps.

#### 1.4.13 Unaligned Accesses

Unaligned memory accesses are not supported by this variant. Set parameter “unaligned” to “T” to enable such accesses.

Unaligned memory accesses are not supported for AMO instructions by this variant. Set parameter “unalignedAMO” to “T” to enable such accesses.

Address misaligned exceptions are higher priority than page fault or access fault exceptions on this variant. Set parameter “unaligned\_low\_pri” to “T” to specify that they are lower priority instead.

#### 1.4.14 PMP

8 PMP entries are implemented by this variant. Use parameter “PMP\_registers” to specify a different number of PMP entries; set the parameter to 0 to disable the PMP unit. The PMP grain size (G) is 0, meaning that PMP regions as small as 4 bytes are implemented. Use parameter “PMP\_grain” to specify a different grain size if required. Unaligned PMP accesses are not decomposed into separate aligned accesses; use parameter “PMP\_decompose” to modify this behavior if required. Parameters to change the write masks for the PMP CSRs are not enabled; use parameter “PMP\_maskparams” to modify this behavior if required. Parameters to change the reset values for the PMP CSRs are not enabled; use parameter “PMP\_initialparams” to modify this behavior if required.

Accesses to unimplemented PMP registers are write-ignored and read as zero on this variant. Set parameter “PMP\_undefined” to True to indicate that such accesses should cause Illegal Instruction exceptions instead.

#### 1.4.15 LR/SC Granule

LR/SC instructions are implemented with a 64-byte reservation granule. A different granule size may be specified using parameter “lr\_sc\_grain”.

## 1.5 Compressed Extension

Standard compressed instructions are present in this variant. Legacy compressed extension features may also be configured using parameters described below. Use parameter “`commcompress_version`” to enable more recent compressed extension features if required.

Parameter `Zcea_version` is used to specify the version of Zcea instructions present. By default, `Zcea_version` is set to “none” in this variant. Updates to this parameter require a commercial product license.

Parameter `Zceb_version` is used to specify the version of Zceb instructions present. By default, `Zceb_version` is set to “none” in this variant. Updates to this parameter require a commercial product license.

Parameter `Zcee_version` is used to specify the version of Zcee instructions present. By default, `Zcee_version` is set to “none” in this variant. Updates to this parameter require a commercial product license.

## 1.6 Privileged Architecture

This variant implements the Privileged Architecture with version specified in the References section of this document. Note that parameter “`priv_version`” can be used to select the required architecture version; see the following sections for detailed information about differences between each supported version.

### 1.6.1 Legacy Version 1.10

1.10 version of May 7 2017.

### 1.6.2 Version 20190608

Stable 1.11 version of June 8 2019, with these changes compared to version 1.10:

- `mcountinhibit` CSR defined;
- pages are never executable in Supervisor mode if page table entry U bit is 1;
- `mstatus.TW` is writable if any lower-level privilege mode is implemented (previously, it was just if Supervisor mode was implemented);

### 1.6.3 Version 20211203

1.12 draft version of December 3 2021, with these changes compared to version 20190608:

- `mstatush`, `mseccfg`, `mseccfgh`, `menvcfg`, `menvcfgh`, `senvcfg`, `henvcfg`, `henvcfgh` and `mconfigptr` CSRs defined;

- xret instructions clear mstatus.MPRV when leaving Machine mode if new mode is less privileged than M-mode;
- maximum number of PMP registers increased to 64;
- data endian is now configurable.

#### **1.6.4 Version 1.12**

Official 1.12 version, identical to 20211203.

#### **1.6.5 Version master**

Unstable master version, currently identical to 1.12.

### **1.7 Unprivileged Architecture**

This variant implements the Unprivileged Architecture with version specified in the References section of this document. Note that parameter “user\_version” can be used to select the required architecture version; see the following sections for detailed information about differences between each supported version.

#### **1.7.1 Legacy Version 2.2**

2.2 version of May 7 2017.

#### **1.7.2 Version 20191213**

Stable 20191213-Base-Ratified version of December 13 2019, with these changes compared to version 2.2:

- floating point fmin/fmax instruction behavior modified to comply with IEEE 754-201x.
- numerous other optional behaviors can be separately enabled using Z-prefixed parameters.

### **1.8 Bit-Manipulation Extension**

This variant implements the Bit-Manipulation extension with version specified in the References section of this document. Note that parameter “bitmanip\_version” can be used to select the required version of this extension. See section “Bit-Manipulation Extension Versions” for detailed information about differences between each supported version.

### 1.8.1 Bit-Manipulation Extension Parameters

Parameter Zbb is used to specify that the base instructions are present. By default, Zbb is set to 1 in this variant. Updates to this parameter require a commercial product license.

Parameter Zba is used to specify that address calculation instructions are present. By default, Zba is set to 1 in this variant. Updates to this parameter require a commercial product license.

Parameter Zbc is used to specify that carryless operation instructions are present. By default, Zbc is set to 0 in this variant. Updates to this parameter require a commercial product license.

Parameter Zbe is used to specify that bit deposit/extract instructions are present. By default, Zbe is set to 0 in this variant. Updates to this parameter require a commercial product license. This parameter is ignored for version 1.0.0, which does not implement that subset.

Parameter Zbf is used to specify that bit field place instructions are present. By default, Zbf is set to 0 in this variant. Updates to this parameter require a commercial product license. This parameter is ignored for version 1.0.0, which does not implement that subset.

Parameter Zbm is used to specify that bit matrix operation instructions are present. By default, Zbm is set to 0 in this variant. Updates to this parameter require a commercial product license. This parameter is ignored for version 1.0.0, which does not implement that subset.

Parameter Zbp is used to specify that permutation instructions are present. By default, Zbp is set to 0 in this variant. Updates to this parameter require a commercial product license. This parameter is ignored for version 1.0.0, which does not implement that subset.

Parameter Zbr is used to specify that CRC32 instructions are present. By default, Zbr is set to 0 in this variant. Updates to this parameter require a commercial product license. This parameter is ignored for version 1.0.0, which does not implement that subset.

Parameter Zbs is used to specify that single bit instructions are present. By default, Zbs is set to 0 in this variant. Updates to this parameter require a commercial product license.

Parameter Zbt is used to specify that ternary instructions are present. By default, Zbt is set to 0 in this variant. Updates to this parameter require a commercial product license. This parameter is ignored for version 1.0.0, which does not implement that subset.

### 1.8.2 Bit-Manipulation Extension Versions

The Bit-Manipulation Extension specification has been under active development. To enable simulation of hardware that may be based on an older version of the specification, the model implements behavior for a number of previous versions of the specification. The differing features of these are listed below, in chronological order.

### 1.8.3 Version 0.90

Stable 0.90 version of June 10 2019.

### 1.8.4 Version 0.91

Stable 0.91 version of August 29 2019, with these changes compared to version 0.90:

- change encodings of bmatxor, grev, grevw, grevi and greviw;
- add gorc, gorcw, gorci, gorciw, bfp and bfpw instructions.

### 1.8.5 Version 0.92

Stable 0.92 version of November 8 2019, with these changes compared to version 0.91:

- add packh, packu and packuw instructions;
- add sext.b and sext.h instructions;
- change encoding and behavior of bfp and bfpw instructions;
- change encoding of bdep and bdepw instructions.

### 1.8.6 Version 0.93-draft

Draft 0.93 version of January 29 2020, with these changes compared to version 0.92:

- add shladd, sh2add, sh3add, shladdu, sh2addu and sh3addu instructions;
- move slo, sloi, sro and sroi to Zbp subset;
- add orc16 to Zbb subset.

### 1.8.7 Version 0.93

Stable 0.93 version of January 10 2021, with these changes compared to version 0.93-draft:

- assignments of instructions to Z extension groups changed;
- exchange encodings of max and minu instructions;
- add xperm.[nbhw] instructions;
- instructions named \*u.w renamed to \*.uw;
- instruction add.uw zero-extends argument rs1, not rs2;
- instructions named sb\* renamed to b\*;
- instructions named pcnt\* renamed to cpop\*;
- instructions subu.w, addiwu, addwu, subwu, clmulw, clmulrw and clmulhw removed;
- instructions slo, sro, sloi, sroi, slow, srow, sloiw and sroiw removed from all Z extension groups and are therefore never implemented;
- instructions bext/bdep renamed to bcompress/bdecompress (this change is documented under the draft 0.94 version but is required to resolve an instruction name conflict introduced by instruction

renames above);

### 1.8.8 Version 0.94

Stable 0.94 version of January 20 2021, with these changes compared to version 0.93:

- instructions bset[i]w, bclr[i]w, binv[i]w and bextw removed.

### 1.8.9 Version 1.0.0

Stable 1.0.0 version of June 6 2021, with these changes compared to version 0.94:

- instructions with immediate shift operands now follow base architecture semantics to determine operand legality instead of masking to XLEN-1;
- only subsets Zba, Zbb, Zbc and Zbs may be enabled;
- if the B extension is present, it is implicitly always enabled and not subject to control by misa.B, which is zero.

### 1.8.10 Version master

Unstable master version, with these changes compared to version 1.0.0:

- any subset may be enabled;
- xperm.n, xperm.b, xperm.h and xperm.w instructions renamed xperm4, xperm8, xperm16 and xperm32.

## 1.9 Other Extensions

Other extensions that can be configured are described in this section.

### 1.9.1 Zmmul

Parameter “Zmmul” is 0 on this variant, meaning that all multiply and divide instructions are implemented. if “Zmmul” is set to 1 then multiply instructions are implemented but divide and remainder instructions are not implemented.

### 1.9.2 Zicsr

Parameter “Zicsr” is 1 on this variant, meaning that standard CSRs and CSR access instructions are implemented. if “Zicsr” is set to 0 then standard CSRs and CSR access instructions are not implemented and an alternative scheme must be provided as a processor extension.

### 1.9.3 Zifencei

Parameter “Zifencei” is 1 on this variant, meaning that the fence.i instruction is implemented (but treated as a NOP by the model). if “Zifencei” is set to 0 then the fence.i instruction is not implemented.

### 1.9.4 Zicbom

Parameter “Zicbom” is 0 on this variant, meaning that code block management instructions are undefined. if “Zicbom” is set to 1 then code block management instructions cbo.clean, cbo.flush and cbo.inval are defined.

If Zicbom is present, the cache block size is given by parameter “cmomp\_bytes”. The instructions may cause traps if used illegally but otherwise are NOPs in this model.

### 1.9.5 Zicbop

Parameter “Zicbop” is 0 on this variant, meaning that prefetch instructions are undefined. if “Zicbop” is set to 1 then prefetch instructions prefetch.i, prefetch.r and prefetch.w are defined (but behave as NOPs in this model).

### 1.9.6 Zicboz

Parameter “Zicboz” is 0 on this variant, meaning that the cbo.zero instruction is undefined. if “Zicboz” is set to 1 then the cbo.zero instruction is defined.

If Zicboz is present, the cache block size is given by parameter “cmoz\_bytes”.

### 1.9.7 Smstateen

Parameter “Smstateen” is 0 on this variant, meaning that state enable CSRs are undefined. if “Smstateen” is set to 1 then state enable CSRs are defined.

Within the state enable CSRs, only bit 1 (for Zfinx), bit 57 (for xcontext CSR access), bit 62 (for xenvcfg CSR access) and bit 63 (for lower-level state enable CSR access) are currently implemented.

## 1.10 Load-Reserved/Store-Conditional Locking

By default, LR/SC locking is implemented automatically by the model and simulator, with a reservation granule defined by the “lr\_sc\_grain” parameter. It is also possible to implement locking externally to the model in a platform component, using the “LR\_address”, “SC\_address” and “SC\_valid” net ports, as described below.

The “LR\_address” output net port is written by the model with the address used by a load-reserved instruction as it executes. This port should be connected as an input to the external lock



management component, which should record the address, and also that an LR/SC transaction is active.

The “SC\_address” output net port is written by the model with the address used by a store-conditional instruction as it executes. This should be connected as an input to the external lock management component, which should compare the address with the previously-recorded load-reserved address, and determine from this (and other implementation-specific constraints) whether the store should succeed. It should then immediately write the Boolean success/fail code to the “SC\_valid” input net port of the model. Finally, it should update state to indicate that an LR/SC transaction is no longer active.

It is also possible to write zero to the “SC\_valid” input net port at any time outside the context of a store-conditional instruction, which will mark any active LR/SC transaction as invalid.

Irrespective of whether LR/SC locking is implemented internally or externally, taking any exception or interrupt or executing exception-return instructions (e.g. MRET) will always mark any active LR/SC transaction as invalid.

Parameter “amo\_aborts\_lr\_sc” is used to specify whether AMO operations abort any active LR/SC pair. In this variant, “amo\_aborts\_lr\_sc” is 0.

## 1.11 Active Atomic Operation Indication

The “AMO\_active” output net port is written by the model with a code indicating any current atomic memory operation while the instruction is active. The written codes are:

- 0: no atomic instruction active
- 1: AMOMIN active
- 2: AMOMAX active
- 3: AMOMINU active
- 4: AMOMAXU active
- 5: AMOADD active
- 6: AMOXOR active
- 7: AMOOR active
- 8: AMOAND active
- 9: AMOSWAP active
- 10: LR active
- 11: SC active

## 1.12 Interrupts

The “reset” port is an active-high reset input. The processor is halted when “reset” goes high and resumes execution from the reset address specified using the “reset\_address” parameter or “reset\_addr” port when the signal goes low. The “mcause” register is cleared to zero.

The “nmi” port is an active-high NMI input. The processor resumes execution from the address specified using the “nmi\_address” parameter or “nmi\_addr” port when the NMI signal goes high. The “mcause” register is cleared to zero.

All other interrupt ports are active high. For each implemented privileged execution level, there are by default input ports for software interrupt, timer interrupt and external interrupt; for example, for Machine mode, these are called “MSWInterrupt”, “MTimerInterrupt” and “MExternalInterrupt”, respectively. When the N extension is implemented, ports are also present for User mode. Parameter “unimp\_int\_mask” allows the default behavior to be changed to exclude certain interrupt ports. The parameter value is a mask in the same format as the “mip” CSR; any interrupt corresponding to a non-zero bit in this mask will be removed from the processor and read as zero in “mip”, “mie” and “mideleg” CSRs (and Supervisor and User mode equivalents if implemented).

Parameter “external\_int\_id” can be used to enable extra interrupt ID input ports on each hart. If the parameter is True then when an external interrupt is applied the value on the ID port is sampled and used to fill the Exception Code field in the “mcause” CSR (or the equivalent CSR for other execution levels). For Machine mode, the extra interrupt ID port is called “MExternalInterruptID”.

The “deferint” port is an active-high artifact input that, when written to 1, prevents any pending-and-enabled interrupt being taken (normally, such an interrupt would be taken on the next instruction after it becomes pending-and-enabled). The purpose of this signal is to enable alignment with hardware models in step-and-compare usage.

## 1.13 Debug Mode

The model can be configured to implement Debug mode using parameter “debug\_mode”. This implements features described in Chapter 4 of the RISC-V External Debug Support specification with version specified by parameter “debug\_version” (see References). Some aspects of this mode are not defined in the specification because they are implementation-specific; the model provides infrastructure to allow implementation of a Debug Module using a custom harness. Features added are described below.

Parameter “debug\_mode” can be used to specify three different behaviors, as follows:

1. If set to value “vector”, then operations that would cause entry to Debug mode result in the processor jumping to the address specified by the “debug\_address” parameter. It will execute at this address, in Debug mode, until a “dret” instruction causes return to non-Debug mode. Any exception generated during this execution will cause a jump to the address specified by the “dexc\_address” parameter.
2. If set to value “interrupt”, then operations that would cause entry to Debug mode result in the processor simulation call (e.g. `opProcessorSimulate`) returning, with a stop reason of `OP_SR_INTERRUPT`. In this usage scenario, the Debug Module is implemented in the simula-

tion harness.

3. If set to value “halt”, then operations that would cause entry to Debug mode result in the processor halting. Depending on the simulation environment, this might cause a return from the simulation call with a stop reason of OP\_SR\_HALT, or debug mode might be implemented by another platform component which then restarts the debugged processor again.

### 1.13.1 Debug State Entry

The specification does not define how Debug mode is implemented. In this model, Debug mode is enabled by a Boolean pseudo-register, “DM”. When “DM” is True, the processor is in Debug mode. When “DM” is False, mode is defined by “mstatus” in the usual way.

Entry to Debug mode can be performed in any of these ways:

1. By writing True to register “DM” (e.g. using opProcessorRegWrite) followed by simulation of at least one cycle (e.g. using opProcessorSimulate), dcsr cause will be reported as trigger;
2. By writing a 1 then 0 to net “haltreq” (using opNetWrite) followed by simulation of at least one cycle (e.g. using opProcessorSimulate);
3. By writing a 1 to net “resethaltreq” (using opNetWrite) while the “reset” signal undergoes a negedge transition, followed by simulation of at least one cycle (e.g. using opProcessorSimulate);
4. By executing an “ebreak” instruction when Debug mode entry for the current processor mode is enabled by dcsr.ebreakm, dcsr.ebreaks or dcsr.ebreaku.

In all cases, the processor will save required state in “dpc” and “dcsr” and then perform actions described above, depending in the value of the “debug\_mode” parameter.

### 1.13.2 Debug State Exit

Exit from Debug mode can be performed in any of these ways:

1. By writing False to register “DM” (e.g. using opProcessorRegWrite) followed by simulation of at least one cycle (e.g. using opProcessorSimulate);
2. By executing an “dret” instruction when Debug mode.

In both cases, the processor will perform the steps described in section 4.6 (Resume) of the Debug specification.

### 1.13.3 Debug Registers

When Debug mode is enabled, registers “dcsr”, “dpc”, “dscratch0” and “dscratch1” are implemented as described in the specification. These may be manipulated externally by a Debug Module using opProcessorRegRead or opProcessorRegWrite; for example, the Debug Module could write “dcsr” to enable “ebreak” instruction behavior as described above, or read and write “dpc” to emulate stepping over an “ebreak” instruction prior to resumption from Debug mode.

### 1.13.4 Debug Mode Execution

The specification allows execution of code fragments in Debug mode. A Debug Module implementation can cause execution in Debug mode by the following steps:

1. Write the address of a Program Buffer to the program counter using `opProcessorPCSet`;
2. If “`debug_mode`” is set to “halt”, write 0 to pseudo-register “DMStall” (to leave halted state);
3. If entry to Debug mode was handled by exiting the simulation callback, call `opProcessorSimulate` or `opRootModuleSimulate` to resume simulation.

Debug mode will be re-entered in these cases:

1. By execution of an “`ebreak`” instruction; or:
2. By execution of an instruction that causes an exception.

In both cases, the processor will either jump to the debug exception address, or return control immediately to the harness, with `stopReason` of `OP_SR_INTERRUPT`, or perform a halt, depending on the value of the “`debug_mode`” parameter.

### 1.13.5 Debug Single Step

When in Debug mode, the processor or harness can cause a single instruction to be executed on return from that mode by setting `dcsr.step`. After one non-Debug-mode instruction has been executed, control will be returned to the harness. The processor will remain in single-step mode until `dcsr.step` is cleared.

### 1.13.6 Debug Event Priorities

The model supports two different models for determining which debug exception occurs when multiple debug events are pending:

- 1: original mode (when parameter “`debug_priority`”=“original”);
- 2: modified mode, as described in Debug Specification pull request 693 (when parameter “`debug_priority`”=“PR693”). This mode resolves some anomalous behavior of the original specification.

### 1.13.7 Debug Ports

Port “DM” is an output signal that indicates whether the processor is in Debug mode

Port “`haltreq`” is a rising-edge-triggered signal that triggers entry to Debug mode (see above).

Port “`resethaltreq`” is a level-sensitive signal that triggers entry to Debug mode after reset (see above).

## 1.14 Debug Mask

It is possible to enable model debug messages in various categories. This can be done statically using the “debugflags” parameter, or dynamically using the “debugflags” command. Enabled messages are specified using a bitmask value, as follows:

Value 0x002: enable debugging of PMP and virtual memory state;

Value 0x004: enable debugging of interrupt state.

All other bits in the debug bitmask are reserved and must not be set to non-zero values.

## 1.15 Integration Support

This model implements a number of non-architectural pseudo-registers and other features to facilitate integration.

### 1.15.1 CSR Register External Implementation

If parameter “enable\_CSR\_bus” is True, an artifact 16-bit bus “CSR” is enabled. Slave callbacks installed on this bus can be used to implement modified CSR behavior (use opBusSlaveNew or icmMapExternalMemory, depending on the client API). A CSR with index 0xABC is mapped on the bus at address 0xABC0; as a concrete example, implementing CSR “time” (number 0xC01) externally requires installation of callbacks at address 0xC010 on the CSR bus.

### 1.15.2 LR/SC Active Address

Artifact register “LRSCAddress” shows the active LR/SC lock address. The register holds all-ones if there is no LR/SC operation active or if LR/SC locking is implemented externally as described above.

## 1.16 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. fence.i) are treated as NOPs, with the exception of any Illegal Instruction behavior, which is modeled.

Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous. Data barrier instructions (e.g. fence) are treated as NOPs, with the exception of any Illegal Instruction behavior, which is modeled.

Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.

Hardware Performance Monitor registers are not implemented and hardwired to zero.

## 1.17 Verification

All instructions have been extensively tested by Imperas, using tests generated specifically for this model and also reference tests from <https://github.com/riscv/riscv-tests>.

Also reference tests have been used from various sources including:

<https://github.com/riscv/riscv-tests>

<https://github.com/ucb-bar/riscv-torture>

The Imperas OVPsim RISC-V models are used in the RISC-V Foundation Compliance Framework as a functional Golden Reference:

<https://github.com/riscv/riscv-compliance>

where the simulated model is used to provide the reference signatures for compliance testing. The Imperas OVPsim RISC-V models are used as reference in both open source and commercial instruction stream test generators for hardware design verification, for example:

<http://valtrix.in/sting> from Valtrix

<https://github.com/google/riscv-dv> from Google

The Imperas OVPsim RISC-V models are also used by commercial and open source RISC-V Core RTL developers as a reference to ensure correct functionality of their IP.

## 1.18 References

The Model details are based upon the following specifications:

RISC-V Instruction Set Manual, Volume I: User-Level ISA (User Architecture Version 20191213)

RISC-V Instruction Set Manual, Volume II: Privileged Architecture (Privileged Architecture Version Ratified-IMFDQC-and-Priv-v1.11)

RISC-V “B” Bit Manipulation Extension (Bit Manipulation Architecture Version v0.94-20210120)

RISC-V Core-Local Interrupt Controller (CLIC Version 20180831)

SiFive S21 Manual v19.05

# Chapter 2

## Configuration

### 2.1 Location

This model's VLNv is [sifive.ovpworld.org/processor/riscv/1.0](http://sifive.ovpworld.org/processor/riscv/1.0).

The model source is usually at:

`$IMPERAS_HOME/ImperasLib/source/sifive.ovpworld.org/processor/riscv/1.0`

The model binary is usually at:

`$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/sifive.ovpworld.org/processor/riscv/1.0`

### 2.2 GDB Path

The default GDB for this model is: `$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/riscv-none-embed-gdb`.

### 2.3 Semi-Host Library

The default semi-host library file is `riscv.ovpworld.org/semihosting/pk/1.0`

### 2.4 Processor Endian-ness

This is a LITTLE endian model.

### 2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

### 2.6 Processor ELF code

The ELF code supported by this model is: 0xf3.

## Chapter 3

# All Variants in this model

This model has these variants

Variant	Description
E20	
E21	
E24	
E31	
E34	
E51	
E76	
S21	(described in this document)
S51	
S54	
S76	
U54	
U74	
X280	
P550	
P650	
P270	
E61	
S61	
U64	

Table 3.1: All Variants in this model



## Chapter 4

# Bus Master Ports

This model has these bus master ports.

<b>Name</b>	min	max	Connect?	Description
INSTRUCTION	32	64	mandatory	Instruction bus
DATA	32	64	optional	Data bus

Table 4.1: Bus Master Ports

## Chapter 5

# Bus Slave Ports

This model has no bus slave ports.

## Chapter 6

# Net Ports

This model has these net ports.

Name	Type	Connect?	Description
hart0_reset	input	optional	Reset
hart0_reset_addr	input	optional	externally-applied reset address
hart0_nmi	input	optional	NMI
hart0_nmi_cause	input	optional	externally-applied NMI cause
hart0_nmi_addr	input	optional	externally-applied NMI address
hart0_nmieuxc_addr	input	optional	externally-applied RNMI exception address
hart0_MSInterrupt	input	optional	Machine software interrupt
hart0_MTimerInterrupt	input	optional	Machine timer interrupt
hart0_MExternalInterrupt	input	optional	Machine external interrupt
hart0_CSIP	input	optional	CLIC software interrupt
hart0_LocalInterrupt0	input	optional	Local interrupt 0
hart0_LocalInterrupt1	input	optional	Local interrupt 1
hart0_LocalInterrupt2	input	optional	Local interrupt 2
hart0_LocalInterrupt3	input	optional	Local interrupt 3
hart0_LocalInterrupt4	input	optional	Local interrupt 4
hart0_LocalInterrupt5	input	optional	Local interrupt 5
hart0_LocalInterrupt6	input	optional	Local interrupt 6
hart0_LocalInterrupt7	input	optional	Local interrupt 7
hart0_LocalInterrupt8	input	optional	Local interrupt 8
hart0_LocalInterrupt9	input	optional	Local interrupt 9
hart0_LocalInterrupt10	input	optional	Local interrupt 10
hart0_LocalInterrupt11	input	optional	Local interrupt 11
hart0_LocalInterrupt12	input	optional	Local interrupt 12
hart0_LocalInterrupt13	input	optional	Local interrupt 13
hart0_LocalInterrupt14	input	optional	Local interrupt 14
hart0_LocalInterrupt15	input	optional	Local interrupt 15
hart0_LocalInterrupt16	input	optional	Local interrupt 16
hart0_LocalInterrupt17	input	optional	Local interrupt 17
hart0_LocalInterrupt18	input	optional	Local interrupt 18
hart0_LocalInterrupt19	input	optional	Local interrupt 19

hart0_LocalInterrupt20	input	optional	Local interrupt 20
hart0_LocalInterrupt21	input	optional	Local interrupt 21
hart0_LocalInterrupt22	input	optional	Local interrupt 22
hart0_LocalInterrupt23	input	optional	Local interrupt 23
hart0_LocalInterrupt24	input	optional	Local interrupt 24
hart0_LocalInterrupt25	input	optional	Local interrupt 25
hart0_LocalInterrupt26	input	optional	Local interrupt 26
hart0_LocalInterrupt27	input	optional	Local interrupt 27
hart0_LocalInterrupt28	input	optional	Local interrupt 28
hart0_LocalInterrupt29	input	optional	Local interrupt 29
hart0_LocalInterrupt30	input	optional	Local interrupt 30
hart0_LocalInterrupt31	input	optional	Local interrupt 31
hart0_LocalInterrupt32	input	optional	Local interrupt 32
hart0_LocalInterrupt33	input	optional	Local interrupt 33
hart0_LocalInterrupt34	input	optional	Local interrupt 34
hart0_LocalInterrupt35	input	optional	Local interrupt 35
hart0_LocalInterrupt36	input	optional	Local interrupt 36
hart0_LocalInterrupt37	input	optional	Local interrupt 37
hart0_LocalInterrupt38	input	optional	Local interrupt 38
hart0_LocalInterrupt39	input	optional	Local interrupt 39
hart0_LocalInterrupt40	input	optional	Local interrupt 40
hart0_LocalInterrupt41	input	optional	Local interrupt 41
hart0_LocalInterrupt42	input	optional	Local interrupt 42
hart0_LocalInterrupt43	input	optional	Local interrupt 43
hart0_LocalInterrupt44	input	optional	Local interrupt 44
hart0_LocalInterrupt45	input	optional	Local interrupt 45
hart0_LocalInterrupt46	input	optional	Local interrupt 46
hart0_LocalInterrupt47	input	optional	Local interrupt 47
hart0_LocalInterrupt48	input	optional	Local interrupt 48
hart0_LocalInterrupt49	input	optional	Local interrupt 49
hart0_LocalInterrupt50	input	optional	Local interrupt 50
hart0_LocalInterrupt51	input	optional	Local interrupt 51
hart0_LocalInterrupt52	input	optional	Local interrupt 52
hart0_LocalInterrupt53	input	optional	Local interrupt 53
hart0_LocalInterrupt54	input	optional	Local interrupt 54
hart0_LocalInterrupt55	input	optional	Local interrupt 55
hart0_LocalInterrupt56	input	optional	Local interrupt 56
hart0_LocalInterrupt57	input	optional	Local interrupt 57
hart0_LocalInterrupt58	input	optional	Local interrupt 58
hart0_LocalInterrupt59	input	optional	Local interrupt 59
hart0_LocalInterrupt60	input	optional	Local interrupt 60
hart0_LocalInterrupt61	input	optional	Local interrupt 61
hart0_LocalInterrupt62	input	optional	Local interrupt 62
hart0_LocalInterrupt63	input	optional	Local interrupt 63
hart0_LocalInterrupt64	input	optional	Local interrupt 64

hart0_LocalInterrupt65	input	optional	Local interrupt 65
hart0_LocalInterrupt66	input	optional	Local interrupt 66
hart0_LocalInterrupt67	input	optional	Local interrupt 67
hart0_LocalInterrupt68	input	optional	Local interrupt 68
hart0_LocalInterrupt69	input	optional	Local interrupt 69
hart0_LocalInterrupt70	input	optional	Local interrupt 70
hart0_LocalInterrupt71	input	optional	Local interrupt 71
hart0_LocalInterrupt72	input	optional	Local interrupt 72
hart0_LocalInterrupt73	input	optional	Local interrupt 73
hart0_LocalInterrupt74	input	optional	Local interrupt 74
hart0_LocalInterrupt75	input	optional	Local interrupt 75
hart0_LocalInterrupt76	input	optional	Local interrupt 76
hart0_LocalInterrupt77	input	optional	Local interrupt 77
hart0_LocalInterrupt78	input	optional	Local interrupt 78
hart0_LocalInterrupt79	input	optional	Local interrupt 79
hart0_LocalInterrupt80	input	optional	Local interrupt 80
hart0_LocalInterrupt81	input	optional	Local interrupt 81
hart0_LocalInterrupt82	input	optional	Local interrupt 82
hart0_LocalInterrupt83	input	optional	Local interrupt 83
hart0_LocalInterrupt84	input	optional	Local interrupt 84
hart0_LocalInterrupt85	input	optional	Local interrupt 85
hart0_LocalInterrupt86	input	optional	Local interrupt 86
hart0_LocalInterrupt87	input	optional	Local interrupt 87
hart0_LocalInterrupt88	input	optional	Local interrupt 88
hart0_LocalInterrupt89	input	optional	Local interrupt 89
hart0_LocalInterrupt90	input	optional	Local interrupt 90
hart0_LocalInterrupt91	input	optional	Local interrupt 91
hart0_LocalInterrupt92	input	optional	Local interrupt 92
hart0_LocalInterrupt93	input	optional	Local interrupt 93
hart0_LocalInterrupt94	input	optional	Local interrupt 94
hart0_LocalInterrupt95	input	optional	Local interrupt 95
hart0_LocalInterrupt96	input	optional	Local interrupt 96
hart0_LocalInterrupt97	input	optional	Local interrupt 97
hart0_LocalInterrupt98	input	optional	Local interrupt 98
hart0_LocalInterrupt99	input	optional	Local interrupt 99
hart0_LocalInterrupt100	input	optional	Local interrupt 100
hart0_LocalInterrupt101	input	optional	Local interrupt 101
hart0_LocalInterrupt102	input	optional	Local interrupt 102
hart0_LocalInterrupt103	input	optional	Local interrupt 103
hart0_LocalInterrupt104	input	optional	Local interrupt 104
hart0_LocalInterrupt105	input	optional	Local interrupt 105
hart0_LocalInterrupt106	input	optional	Local interrupt 106
hart0_LocalInterrupt107	input	optional	Local interrupt 107
hart0_LocalInterrupt108	input	optional	Local interrupt 108
hart0_LocalInterrupt109	input	optional	Local interrupt 109

hart0_LocalInterrupt110	input	optional	Local interrupt 110
hart0_LocalInterrupt111	input	optional	Local interrupt 111
hart0_LocalInterrupt112	input	optional	Local interrupt 112
hart0_LocalInterrupt113	input	optional	Local interrupt 113
hart0_LocalInterrupt114	input	optional	Local interrupt 114
hart0_LocalInterrupt115	input	optional	Local interrupt 115
hart0_LocalInterrupt116	input	optional	Local interrupt 116
hart0_LocalInterrupt117	input	optional	Local interrupt 117
hart0_LocalInterrupt118	input	optional	Local interrupt 118
hart0_LocalInterrupt119	input	optional	Local interrupt 119
hart0_LocalInterrupt120	input	optional	Local interrupt 120
hart0_LocalInterrupt121	input	optional	Local interrupt 121
hart0_LocalInterrupt122	input	optional	Local interrupt 122
hart0_LocalInterrupt123	input	optional	Local interrupt 123
hart0_LocalInterrupt124	input	optional	Local interrupt 124
hart0_LocalInterrupt125	input	optional	Local interrupt 125
hart0_LocalInterrupt126	input	optional	Local interrupt 126
hart0_irq_ack_o	output	optional	interrupt acknowledge (pulse)
hart0_irq_id_o	output	optional	acknowledged interrupt id (valid during irq_ack_o pulse)
hart0_sec_lvl_o	output	optional	current privilege level
hart0_LR_address	output	optional	Port written with effective address for LR instruction
hart0_SC_address	output	optional	Port written with effective address for SC instruction
hart0_SC_valid	input	optional	SC.address valid input signal
hart0_AMO_active	output	optional	Port written with code indicating active AMO
hart0_deferint	input	optional	Artifact signal causing interrupts to be held off when high

Table 6.1: Net Ports

## Chapter 7

# FIFO Ports

This model has no FIFO ports.

# Chapter 8

## Formal Parameters

Name	Type	Description
<b>Fundamental</b>		
variant	Enumeration	Selects variant (either a generic UISA or a specific model)
user_version	Enumeration	Specify required User Architecture version (2.2, 2.3, 20190305 or 20191213)
priv_version	Enumeration	Specify required Privileged Architecture version (1.10, 1.11, 20190405, 20190608, 20211203, 1.12 or master)
numHarts	Uns32	Specify the number of hart contexts in a multiprocessor
endian	Endian	Model endian
enable_expanded	Boolean	Specify that 48-bit and 64-bit expanded instructions are supported
endianFixed	Boolean	Specify that data endianness is fixed (mstatus.{MBE,SBE,UBE} fields are read-only)
misa_MXL	Uns32	Override default value of misa.MXL
misa_Extensions	Uns32	Override default value of misa.Extensions
add_Extensions	String	Add extensions specified by letters to misa.Extensions (for example, specify “VD” to add V and D features)
sub_Extensions	String	Remove extensions specified by letters from misa.Extensions (for example, specify “VD” to remove V and D features)
misa_Extensions_mask	Uns32	Override mask of writable bits in misa.Extensions
add_Extensions_mask	String	Add extensions specified by letters to mask of writable bits in misa.Extensions (for example, specify “VD” to add V and D features)
sub_Extensions_mask	String	Remove extensions specified by letters from mask of writable bits in misa.Extensions (for example, specify “VD” to remove V and D features)
add_implicit_Extensions	String	Add extensions specified by letters to implicitly-present extensions not visible in misa.Extensions
sub_implicit_Extensions	String	Remove extensions specified by letters from implicitly-present extensions not visible in misa.Extensions
<b>Bit_Manipulation_Extension</b>		
bitmanip_version	Enumeration	Specify required Bit Manipulation Architecture version (0.90, 0.91, 0.92, 0.93-draft, 0.93, 0.94, 1.0.0 or master)
Zba	Boolean	Specify that Zba is implemented
Zbb	Boolean	Specify that Zbb is implemented
Zbc	Boolean	Specify that Zbc is implemented
Zbe	Boolean	Specify that Zbe is implemented (ignored if version 1.0.0)
Zbf	Boolean	Specify that Zbf is implemented (ignored if version 1.0.0)
Zbm	Boolean	Specify that Zbm is implemented (ignored if version 1.0.0)
Zbp	Boolean	Specify that Zbp is implemented (ignored if version 1.0.0)
Zbr	Boolean	Specify that Zbr is implemented (ignored if version 1.0.0)
Zbs	Boolean	Specify that Zbs is implemented
Zbt	Boolean	Specify that Zbt is implemented (ignored if version 1.0.0)
<b>Compressed_Extension</b>		



compress_version	Enumeration	Specify required Compressed Architecture version (legacy, 0.70.1 or 0.70.5)
Zcea_version	Enumeration	Specify version of Zcea implemented (legacy only) (none or 0.50.1)
Zceb_version	Enumeration	Specify version of Zceb implemented (legacy only) (none or 0.50.1)
Zcee_version	Enumeration	Specify version of Zcee implemented (legacy only) (none or 1.0.0-rc)
<b>Interrupts_Exceptions</b>		
rnmi_version	Enumeration	Specify required RNMI Architecture version (none or 0.2.1)
mtvec_is_ro	Boolean	Specify whether mtvec CSR is read-only
tvec_align	Uns32	Specify hardware-enforced alignment of mtvec/stvec/utvec when Vectored interrupt mode enabled
ecode_mask	Uns64	Specify hardware-enforced mask of writable bits in xcause.ExceptionCode
ecode_nmi	Uns64	Specify xcause.ExceptionCode for NMI
ecode_nmi_mask	Uns64	Specify hardware-enforced mask of writable bits in mn-cause.ExceptionCode
nmi_is_latched	Boolean	Specify whether NMI input is latched on rising edge (if False, it is level-sensitive)
tval_zero	Boolean	Specify whether mtval/stval/utval are hard wired to zero
tval_zero_ebreak	Boolean	Specify whether mtval/stval/utval are set to zero by an ebreak
tval_ii_code	Boolean	Specify whether mtval/stval contain faulting instruction bits on illegal instruction exception
trap_preserves_lr	Boolean	Whether a trap preserves active LR/SC state
xret_preserves_lr	Boolean	Whether an xret instruction preserves active LR/SC state
reset_address	Uns64	Override reset vector address
nmi_address	Uns64	Override NMI vector address
nmiexc_address	Uns64	Override RNMI exception vector address
CLINT_address	Uns64	Specify base address of internal CLINT model (or 0 for no CLINT)
mtime_Hz	Double	Specify clock frequency of CLINT mtime counter
local_int_num	Uns32	Specify number of supplemental local interrupts
unimp_int_mask	Uns64	Specify mask of unimplemented interrupts (e.g. 1<<9 indicates Supervisor external interrupt unimplemented)
force_mideleg	Uns64	Specify mask of interrupts always delegated to lower-priority execution level from Machine execution level
no_ideleg	Uns64	Specify mask of interrupts that cannot be delegated to lower-priority execution levels
no_e deleg	Uns64	Specify mask of exceptions that cannot be delegated to lower-priority execution levels
external_int_id	Boolean	Whether to add nets allowing External Interrupt ID codes to be forced
<b>Fast Interrupt</b>		
CLIC_version	Enumeration	Specify required CLIC version (20180831, 0.9-draft-20191208, 0.9-draft-20220315 or master)
mclicbase	Uns64	Override mclicbase register
CLICLEVELS	Uns32	Specify number of interrupt levels implemented by CLIC, or 0 if CLIC absent
CLICANDBASIC	Boolean	Whether original basic mode is also implemented
CLICVERSION	Uns32	Specify CLIC version
CLICINTCTLBITS	Uns32	Specify number of bits implemented in clicintctl[i]
CLICCFGLBITS	Uns32	Specify number of bits implemented for cliccfg.nbits
CLICSELHVEC	Boolean	Whether selective hardware vectoring supported
CLICXNXTI	Boolean	Whether xnxti CSRs implemented
CLICXCSW	Boolean	Whether xscratchcsw/xscratchcswl CSRs implemented
externalCLIC	Boolean	Whether CLIC is implemented externally (if False, then use implementation in this model)
tvt_undefined	Boolean	Specify that mtvt, stvt and utvt CSRs are undefined
intthresh_undefined	Boolean	Specify that minthresh, sintthresh and uintthresh CSRs are undefined
mclicbase_undefined	Boolean	Specify that mclicbase CSR is undefined
posedge_0_63	Uns64	Mask of interrupts 0 to 63 that are fixed positive edge triggered

poslevel_0_63	Uns64	Mask of interrupts 0 to 63 that are fixed positive level triggered
posedge_other	Boolean	Whether interrupts 64 and above are fixed positive edge triggered
poslevel_other	Boolean	Whether interrupts 64 and above are fixed positive level triggered
<b>Debug_Extension</b>		
debug_mode	Enumeration	Specify how Debug mode is implemented (none, vector, interrupt or halt)
lr_sc_constraint	Enumeration	Specify memory constraint for LR/SC instructions (none, user1 or user2)
amo_constraint	Enumeration	Specify memory constraint for AMO instructions (none, user1 or user2)
<b>Simulation_Artifact</b>		
use_hw_reg_names	Boolean	Specify whether to use hardware register names x0-x31 and f0-f31 instead of ABI register names
no_pseudo_inst	Boolean	Specify whether pseudo-instructions should not be reported in trace and disassembly
verbose	Boolean	Specify verbose output messages
traceVolatile	Boolean	Specify whether volatile registers (e.g. minstret) should be shown in change trace
enable_CSR_bus	Boolean	Add artifact CSR bus port, allowing CSR registers to be externally implemented
CSR_remap	String	Comma-separated list of CSR number mappings, each of the form <csr-Name>=<number>
<b>Memory</b>		
unaligned_low_pri	Boolean	Specify whether address misaligned exceptions are lower priority than page or access fault exceptions
unaligned	Boolean	Specify whether the processor supports unaligned memory accesses
unalignedAMO	Boolean	Specify whether the processor supports unaligned memory accesses for AMO instructions
amo_aborts_lr_sc	Boolean	Specify whether AMO operations abort any active LR/SC pair
lr_sc_grain	Uns32	Specify byte granularity of ll/sc lock region (constrained to a power of two)
<b>Instruction_CSR_Behavior</b>		
wfi_is_nop	Boolean	Specify whether WFI should be treated as a NOP (if not, halt while waiting for interrupts)
counteren_mask	Uns32	Specify hardware-enforced mask of writable bits in mcounteren/scounteren registers
noinhibit_mask	Uns32	Specify hardware-enforced mask of always-zero bits in mcountinhibit register
cycle_undefined	Boolean	Specify that the cycle CSR is undefined
mcycle_undefined	Boolean	Specify that the mcycle CSR is undefined
time_undefined	Boolean	Specify that the time CSR is undefined
instret_undefined	Boolean	Specify that the instret CSR is undefined
minstret_undefined	Boolean	Specify that the minstret CSR is undefined
hpmcounter_undefined	Boolean	Specify that the hpmcounter CSRs are undefined
mhpmcounter_undefined	Boolean	Specify that the mhpmcounter CSRs are undefined
<b>CSR_Masks</b>		
mtvec_mask	Uns64	Specify hardware-enforced mask of writable bits in mtvec register
mtvt_mask	Uns64	Specify hardware-enforced mask of writable bits in CLIC mtvt register
mip_mask	Uns64	Specify hardware-enforced mask of writable bits in mip register
mtvec_sext	Boolean	Specify whether mtvec is sign-extended from most-significant bit
mtvt_sext	Boolean	Specify whether mtvt is sign-extended from most-significant bit
MXL_writable	Boolean	Specify that misa.MXL is writable (feature under development)
UXL_writable	Boolean	Specify that mstatus.UXL is writable (feature under development)
<b>Trigger</b>		
trigger_num	Uns32	Specify the number of implemented hardware triggers
<b>PMP Configuration</b>		
PMP_grain	Uns32	Specify PMP region granularity, G (0 =>4 bytes, 1 =>8 bytes, etc)
PMP_registers	Uns32	Specify the number of implemented PMP address registers

PMP_max_page	Uns32	Specify the maximum size of PMP region to map if non-zero (may improve performance; constrained to a power of two)
PMP_decompose	Boolean	Whether unaligned PMP accesses are decomposed into separate aligned accesses
PMP_undefined	Boolean	Whether accesses to unimplemented PMP registers are undefined (if True) or write ignored and zero (if False)
PMP_maskparams	Boolean	Enable parameters to change the read-only masks for PMP CSRs
PMP_initialparams	Boolean	Enable parameters to change the reset values for PMP CSRs
<b>Other Extensions</b>		
Smstateen	Boolean	Specify that Smstateen is implemented
Zicsr	Boolean	Specify that Zicsr is implemented
Zifencei	Boolean	Specify that Zifencei is implemented
Zicbom	Boolean	Specify that Zicbom is implemented
Zicbop	Boolean	Specify that Zicbop is implemented
Zicboz	Boolean	Specify that Zicboz is implemented
Zmmul	Boolean	Specify that Zmmul is implemented
<b>CSR Defaults</b>		
mvendorid	Uns64	Override mvendorid register
marchid	Uns64	Override marchid register
mimpid	Uns64	Override mimpid register
mhartid	Uns64	Override mhartid register (or first mhartid of an incrementing sequence if this is an SMP variant)
mtvec	Uns64	Override mtvec register

Table 8.1: Parameters that can be set in: SMP

## 8.1 Extension Parameters

Name	Type	Description
FeatureDisable_Present	Boolean	Specify whether Feature Disable CSR present
BranchPredictionMode_Present	Boolean	Specify whether Branch Prediction Mode CSR present
PowerDial_Present	Boolean	Specify whether PowerDial CSR present
CFLUSH_Present	Boolean	Specify whether CFLUSH.D.L1 and CDISCARD.D.L1 instructions present
CEASE_Present	Boolean	Specify whether CEASE instruction present
PAUSE_Present	Boolean	Specify whether PAUSE instruction present

Table 8.2: Parameters for sifiveExtensions

## 8.2 Parameters with enumerated types

### 8.2.1 Parameter user\_version

Set to this value	Description
2.2	User Architecture Version 2.2
2.3	Deprecated and equivalent to 20191213
20190305	Deprecated and equivalent to 20191213
20191213	User Architecture Version 20191213

Table 8.3: Values for Parameter user\_version

### 8.2.2 Parameter priv\_version

Set to this value	Description
1.10	Privileged Architecture Version 1.10
1.11	Privileged Architecture Version 1.11, equivalent to 20190608
20190405	Deprecated and equivalent to 20190608
20190608	Privileged Architecture Version Ratified-IMFDQC-and-Priv-v1.11
20211203	Privileged Architecture Version 20211203
1.12	Privileged Architecture Version 1.12, equivalent to 20211203
master	Privileged Architecture Master Branch as of commit 6bdeb58 (this is subject to change)

Table 8.4: Values for Parameter priv\_version

### 8.2.3 Parameter bitmanip\_version

Set to this value	Description
0.90	Bit Manipulation Architecture Version v0.90-20190610
0.91	Bit Manipulation Architecture Version v0.91-20190829
0.92	Bit Manipulation Architecture Version v0.92-20191108
0.93-draft	Bit Manipulation Architecture Version 0.93-draft-20200129
0.93	Bit Manipulation Architecture Version v0.93-20210110
0.94	Bit Manipulation Architecture Version v0.94-20210120
1.0.0	Bit Manipulation Architecture Version 1.0.0
master	Bit Manipulation Master Branch as of commit 1f56afe (this is subject to change)

Table 8.5: Values for Parameter bitmanip\_version

### 8.2.4 Parameter compress\_version

Set to this value	Description
legacy	Compressed Architecture absent or legacy version
0.70.1	Compressed Architecture Version 0.70.1
0.70.5	Compressed Architecture Version 0.70.5

Table 8.6: Values for Parameter compress\_version

### 8.2.5 Parameter rnmi\_version

Set to this value	Description
none	RNMI not implemented
0.2.1	RNMI version 0.2.1

Table 8.7: Values for Parameter rnmi\_version

### 8.2.6 Parameter CLIC\_version

Set to this value	Description
20180831	CLIC Version 20180831
0.9-draft-20191208	CLIC Version 0.9-draft-20191208
0.9-draft-2020315	CLIC Version 0.9-draft-2020315
master	CLIC Master Branch as of commit 9af754e (this is subject to change)

Table 8.8: Values for Parameter CLIC\_version

### 8.2.7 Parameter debug\_mode

Set to this value	Description
none	Debug mode not implemented
vector	Debug mode implemented by execution at vector
interrupt	Debug mode implemented by interrupt
halt	Debug mode implemented by halt

Table 8.9: Values for Parameter debug\_mode

### 8.2.8 Parameter lr\_sc\_constraint

Set to this value	Description
none	Memory access not constrained
user1	Memory access constrained by MEM_CONSTRAINT_USER1
user2	Memory access constrained by MEM_CONSTRAINT_USER2

Table 8.10: Values for Parameter lr\_sc\_constraint

### 8.2.9 Parameter amo\_constraint

Set to this value	Description
none	Memory access not constrained
user1	Memory access constrained by MEM_CONSTRAINT_USER1
user2	Memory access constrained by MEM_CONSTRAINT_USER2

Table 8.11: Values for Parameter amo\_constraint

### 8.2.10 Parameter Zcea\_version

Set to this value	Description
none	Zcea not implemented
0.50.1	Zcea version 0.50.1

Table 8.12: Values for Parameter Zcea\_version

### 8.2.11 Parameter Zceb\_version

Set to this value	Description
none	Zceb not implemented
0.50.1	Zceb version 0.50.1

Table 8.13: Values for Parameter Zceb\_version

### 8.2.12 Parameter Zcee\_version

Set to this value	Description
none	Zcee not implemented
1.0.0-rc	Zcee version 1.0.0-rc

Table 8.14: Values for Parameter Zcee\_version

## 8.3 Parameter values

These are the current parameter values.

Name	Value
<b>Fundamental</b>	
variant	S21
user_version	20191213
priv_version	20190608
numHarts	1
endian	none
enable_expanded	F
endianFixed	F
misa_MXL	2
misa_Extensions	0x101107
add_Extensions	
sub_Extensions	
misa_Extensions_mask	0
add_Extensions_mask	
sub_Extensions_mask	
add_implicit_Extensions	
sub_implicit_Extensions	
<b>Bit Manipulation Extension</b>	
bitmanip_version	0.94
Zba	T
Zbb	T
Zbc	F
Zbe	F
Zbf	F
Zbm	F
Zbp	F
Zbr	F
Zbs	F
Zbt	F
<b>Compressed Extension</b>	
compress_version	legacy
Zcea_version	none
Zceb_version	none
Zcee_version	none
<b>Interrupts Exceptions</b>	
rnmi_version	0.2.1
mtvec_is_ro	F
tvec_align	64
ecode_mask	31
ecode_nmi	2
ecode_nmi_mask	3
nmi_is_latched	F

tval_zero	F
tval_zero_ebreak	F
tval_ii_code	T
trap_preserves_lr	F
xret_preserves_lr	F
reset_address	0
nmi_address	0
nmiexc_address	0
CLINT_address	0x2000000
mtime_Hz	3.276800e+04
local_int_num	127
unimp_int_mask	0
force_mideleg	0
no_ideleg	0
no_e deleg	0
external_int_id	F
<b>Fast Interrupt</b>	
CLIC_version	20180831
mclicbase	0x2800000
CLICLEVELS	16
CLICANDBASIC	T
CLICVERSION	17
CLICINTCTLBITS	5
CLICCFGLBITS	2
CLICSELHVEC	T
CLICXNXTI	T
CLICXCSW	F
externalCLIC	F
tvtt_undefined	F
intthresh_undefined	T
mclicbase_undefined	T
posedge_0_63	0x100f
poslevel_0_63	0
posedge_other	F
poslevel_other	F
<b>Debug Extension</b>	
debug_mode	none
lr_sc_constraint	user1
amo_constraint	user1
<b>Simulation Artifact</b>	
use_hw_reg_names	F
no_pseudo_inst	F
verbose	F
traceVolatile	F
enable_CSR_bus	F

CSR_remap	
<b>Memory</b>	
unaligned_low_pri	F
unaligned	F
unalignedAMO	F
amo_aborts_lr_sc	F
lr_sc_grain	64
<b>Instruction_CSR_Behavior</b>	
wfi_is_nop	F
counteren_mask	0xffffffff
noinhibit_mask	0
cycle_undefined	F
mcycle_undefined	F
time_undefined	T
instret_undefined	F
minstret_undefined	F
hpmcounter_undefined	F
mhpmcounter_undefined	F
<b>CSR_Masks</b>	
mtvec_mask	0x3fffffff
mtvt_mask	0xffffffffffffc0
mip_mask	0x337
mtvec_sext	F
mtvt_sext	F
MXL_writable	F
UXL_writable	F
<b>Trigger</b>	
trigger_num	0
<b>PMP Configuration</b>	
PMP_grain	0
PMP_registers	8
PMP_max_page	0
PMP_decompose	F
PMP_undefined	F
PMP_maskparams	F
PMP_initialparams	F
<b>Other Extensions</b>	
Smstateen	F
Zicsr	T
Zifencei	T
Zicbom	F
Zicbop	F
Zicboz	F
Zmmul	F
<b>CSR Defaults</b>	



mvendorid	0x489
marchid	0x80000002
mimpid	0x4210427
mhartid	0
mtvec	0
<b>sifiveExtensions</b>	
FeatureDisable_Present*	F
BranchPredictionMode_Present*	F
PowerDial_Present*	F
CFLUSH_Present*	F
CEASE_Present*	F
PAUSE_Present*	F

Table 8.15: Parameter values

\* Parameters marked with an asterisk are part of the processor extension library.

## Chapter 9

# Execution Modes

Mode	Code	Description
User	0	User mode
Machine	3	Machine mode

Table 9.1: Modes implemented in: Hart

## Chapter 10

# Exceptions

Exception	Code	Description
InstructionAddressMisaligned	0	Fetch from unaligned address
InstructionAccessFault	1	No access permission for fetch
IllegalInstruction	2	Undecoded, unimplemented or disabled instruction
Breakpoint	3	EBREAK instruction executed
LoadAddressMisaligned	4	Load from unaligned address
LoadAccessFault	5	No access permission for load
StoreAMOAddressMisaligned	6	Store/atomic memory operation at unaligned address
StoreAMOAccessFault	7	No access permission for store/atomic memory operation
EnvironmentCallFromUMode	8	ECALL instruction executed in User mode
EnvironmentCallFromMMode	11	ECALL instruction executed in Machine mode
InstructionPageFault	12	Page fault at fetch address
LoadPageFault	13	Page fault at load address
StoreAMOPageFault	15	Page fault at store/atomic memory operation address
MSWInterrupt	67	Machine software interrupt
MTimerInterrupt	71	Machine timer interrupt
MExternalInterrupt	75	Machine external interrupt
CSIP	76	CLIC software interrupt
LocalInterrupt0	80	Local interrupt 0
LocalInterrupt1	81	Local interrupt 1
LocalInterrupt2	82	Local interrupt 2
LocalInterrupt3	83	Local interrupt 3
LocalInterrupt4	84	Local interrupt 4
LocalInterrupt5	85	Local interrupt 5
LocalInterrupt6	86	Local interrupt 6
LocalInterrupt7	87	Local interrupt 7
LocalInterrupt8	88	Local interrupt 8
LocalInterrupt9	89	Local interrupt 9
LocalInterrupt10	90	Local interrupt 10

LocalInterrupt11	91	Local interrupt 11
LocalInterrupt12	92	Local interrupt 12
LocalInterrupt13	93	Local interrupt 13
LocalInterrupt14	94	Local interrupt 14
LocalInterrupt15	95	Local interrupt 15
LocalInterrupt16	96	Local interrupt 16
LocalInterrupt17	97	Local interrupt 17
LocalInterrupt18	98	Local interrupt 18
LocalInterrupt19	99	Local interrupt 19
LocalInterrupt20	100	Local interrupt 20
LocalInterrupt21	101	Local interrupt 21
LocalInterrupt22	102	Local interrupt 22
LocalInterrupt23	103	Local interrupt 23
LocalInterrupt24	104	Local interrupt 24
LocalInterrupt25	105	Local interrupt 25
LocalInterrupt26	106	Local interrupt 26
LocalInterrupt27	107	Local interrupt 27
LocalInterrupt28	108	Local interrupt 28
LocalInterrupt29	109	Local interrupt 29
LocalInterrupt30	110	Local interrupt 30
LocalInterrupt31	111	Local interrupt 31
LocalInterrupt32	112	Local interrupt 32
LocalInterrupt33	113	Local interrupt 33
LocalInterrupt34	114	Local interrupt 34
LocalInterrupt35	115	Local interrupt 35
LocalInterrupt36	116	Local interrupt 36
LocalInterrupt37	117	Local interrupt 37
LocalInterrupt38	118	Local interrupt 38
LocalInterrupt39	119	Local interrupt 39
LocalInterrupt40	120	Local interrupt 40
LocalInterrupt41	121	Local interrupt 41
LocalInterrupt42	122	Local interrupt 42
LocalInterrupt43	123	Local interrupt 43
LocalInterrupt44	124	Local interrupt 44
LocalInterrupt45	125	Local interrupt 45
LocalInterrupt46	126	Local interrupt 46
LocalInterrupt47	127	Local interrupt 47
LocalInterrupt48	128	Local interrupt 48
LocalInterrupt49	129	Local interrupt 49
LocalInterrupt50	130	Local interrupt 50
LocalInterrupt51	131	Local interrupt 51
LocalInterrupt52	132	Local interrupt 52
LocalInterrupt53	133	Local interrupt 53
LocalInterrupt54	134	Local interrupt 54
LocalInterrupt55	135	Local interrupt 55

LocalInterrupt56	136	Local interrupt 56
LocalInterrupt57	137	Local interrupt 57
LocalInterrupt58	138	Local interrupt 58
LocalInterrupt59	139	Local interrupt 59
LocalInterrupt60	140	Local interrupt 60
LocalInterrupt61	141	Local interrupt 61
LocalInterrupt62	142	Local interrupt 62
LocalInterrupt63	143	Local interrupt 63
LocalInterrupt64	144	Local interrupt 64
LocalInterrupt65	145	Local interrupt 65
LocalInterrupt66	146	Local interrupt 66
LocalInterrupt67	147	Local interrupt 67
LocalInterrupt68	148	Local interrupt 68
LocalInterrupt69	149	Local interrupt 69
LocalInterrupt70	150	Local interrupt 70
LocalInterrupt71	151	Local interrupt 71
LocalInterrupt72	152	Local interrupt 72
LocalInterrupt73	153	Local interrupt 73
LocalInterrupt74	154	Local interrupt 74
LocalInterrupt75	155	Local interrupt 75
LocalInterrupt76	156	Local interrupt 76
LocalInterrupt77	157	Local interrupt 77
LocalInterrupt78	158	Local interrupt 78
LocalInterrupt79	159	Local interrupt 79
LocalInterrupt80	160	Local interrupt 80
LocalInterrupt81	161	Local interrupt 81
LocalInterrupt82	162	Local interrupt 82
LocalInterrupt83	163	Local interrupt 83
LocalInterrupt84	164	Local interrupt 84
LocalInterrupt85	165	Local interrupt 85
LocalInterrupt86	166	Local interrupt 86
LocalInterrupt87	167	Local interrupt 87
LocalInterrupt88	168	Local interrupt 88
LocalInterrupt89	169	Local interrupt 89
LocalInterrupt90	170	Local interrupt 90
LocalInterrupt91	171	Local interrupt 91
LocalInterrupt92	172	Local interrupt 92
LocalInterrupt93	173	Local interrupt 93
LocalInterrupt94	174	Local interrupt 94
LocalInterrupt95	175	Local interrupt 95
LocalInterrupt96	176	Local interrupt 96
LocalInterrupt97	177	Local interrupt 97
LocalInterrupt98	178	Local interrupt 98
LocalInterrupt99	179	Local interrupt 99
LocalInterrupt100	180	Local interrupt 100

LocalInterrupt101	181	Local interrupt 101
LocalInterrupt102	182	Local interrupt 102
LocalInterrupt103	183	Local interrupt 103
LocalInterrupt104	184	Local interrupt 104
LocalInterrupt105	185	Local interrupt 105
LocalInterrupt106	186	Local interrupt 106
LocalInterrupt107	187	Local interrupt 107
LocalInterrupt108	188	Local interrupt 108
LocalInterrupt109	189	Local interrupt 109
LocalInterrupt110	190	Local interrupt 110
LocalInterrupt111	191	Local interrupt 111
LocalInterrupt112	192	Local interrupt 112
LocalInterrupt113	193	Local interrupt 113
LocalInterrupt114	194	Local interrupt 114
LocalInterrupt115	195	Local interrupt 115
LocalInterrupt116	196	Local interrupt 116
LocalInterrupt117	197	Local interrupt 117
LocalInterrupt118	198	Local interrupt 118
LocalInterrupt119	199	Local interrupt 119
LocalInterrupt120	200	Local interrupt 120
LocalInterrupt121	201	Local interrupt 121
LocalInterrupt122	202	Local interrupt 122
LocalInterrupt123	203	Local interrupt 123
LocalInterrupt124	204	Local interrupt 124
LocalInterrupt125	205	Local interrupt 125
LocalInterrupt126	206	Local interrupt 126

Table 10.1: Exceptions implemented in: Hart

# Chapter 11

## Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

### 11.1 Level 1: SMP

This level in the model hierarchy has 2 commands.

This level in the model hierarchy has no register groups.

This level in the model hierarchy has one child:

hart0

### 11.2 Level 2: Hart

This level in the model hierarchy has 5 commands.

This level in the model hierarchy has 5 register groups:

Group name	Registers
Core	33
User_Control_and_Status	31
Machine_Control_and_Status	100
CLINT	3
Integration_support	12

Table 11.1: Register groups

This level in the model hierarchy has no children.

# Chapter 12

## Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

### 12.1 Level 1: SMP

#### 12.1.1 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.1: isync command arguments

#### 12.1.2 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Argument can be any combination of X (execute), A (load or store access) and S (system)
-mode	Boolean	show processor mode changes
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

Table 12.2: itrace command arguments



## 12.2 Level 2: Hart

### 12.2.1 debugflags

show or modify the processor debug flags

Argument	Type	Description
-get	Boolean	print current processor flags value
-mask	Boolean	print valid debug flag bits
-set	Int32	new processor flags (only flags 0x00000006 can be modified)

Table 12.3: debugflags command arguments

### 12.2.2 getCSRIndex

Return index for a named CSR (or -1 if no matching CSR)

Argument	Type	Description
-name	String	CSR name

Table 12.4: getCSRIndex command arguments

### 12.2.3 isync

specify instruction address range for synchronous execution

Argument	Type	Description
-addresshi	Uns64	end address of synchronous execution range
-addresslo	Uns64	start address of synchronous execution range

Table 12.5: isync command arguments

### 12.2.4 itrace

enable or disable instruction tracing

Argument	Type	Description
-after	Uns64	apply after this many instructions
-enable	Boolean	enable instruction tracing
-instructioncount	Boolean	include the instruction number in each trace
-memory	String	show memory accesses by this instruction. Argument can be any combination of X (execute), A (load or store access) and S (system)
-mode	Boolean	show processor mode changes
-off	Boolean	disable instruction tracing
-on	Boolean	enable instruction tracing
-processorname	Boolean	Include processor name in all trace lines
-registerchange	Boolean	show registers changed by this instruction
-registers	Boolean	show registers after each trace

---

Table 12.6: itrace command arguments

### **12.2.5 listCSRs**

#### **12.2.5.1 Argument description**

List all CSRs in index order

# Chapter 13

## Registers

### 13.1 Level 1: SMP

No registers.

### 13.2 Level 2: Hart

#### 13.2.1 Core

Registers at level:2, type:Hart group:Core

Name	Bits	Initial-Hex	RW	Description
zero	64	0	r-	
ra	64	0	rw	
sp	64	0	rw	stack pointer
gp	64	0	rw	
tp	64	0	rw	
t0	64	0	rw	
t1	64	0	rw	
t2	64	0	rw	
s0	64	0	rw	
s1	64	0	rw	
a0	64	0	rw	
a1	64	0	rw	
a2	64	0	rw	
a3	64	0	rw	
a4	64	0	rw	
a5	64	0	rw	
a6	64	0	rw	
a7	64	0	rw	
s2	64	0	rw	
s3	64	0	rw	
s4	64	0	rw	
s5	64	0	rw	
s6	64	0	rw	
s7	64	0	rw	
s8	64	0	rw	
s9	64	0	rw	
s10	64	0	rw	
s11	64	0	rw	

t3	64	0	rw	
t4	64	0	rw	
t5	64	0	rw	
t6	64	0	rw	
pc	64	0	rw	program counter

Table 13.1: Registers at level 2, type:Hart group:Core

### 13.2.2 User\_Control\_and\_Status

Registers at level:2, type:Hart group:User\_Control\_and\_Status

Name	Bits	Initial-Hex	RW	Description
cycle	64	0	r-	Cycle Counter
instret	64	0	r-	Instructions Retired
hpmcounter3	64	0	r-	Performance Monitor Counter 3
hpmcounter4	64	0	r-	Performance Monitor Counter 4
hpmcounter5	64	0	r-	Performance Monitor Counter 5
hpmcounter6	64	0	r-	Performance Monitor Counter 6
hpmcounter7	64	0	r-	Performance Monitor Counter 7
hpmcounter8	64	0	r-	Performance Monitor Counter 8
hpmcounter9	64	0	r-	Performance Monitor Counter 9
hpmcounter10	64	0	r-	Performance Monitor Counter 10
hpmcounter11	64	0	r-	Performance Monitor Counter 11
hpmcounter12	64	0	r-	Performance Monitor Counter 12
hpmcounter13	64	0	r-	Performance Monitor Counter 13
hpmcounter14	64	0	r-	Performance Monitor Counter 14
hpmcounter15	64	0	r-	Performance Monitor Counter 15
hpmcounter16	64	0	r-	Performance Monitor Counter 16
hpmcounter17	64	0	r-	Performance Monitor Counter 17
hpmcounter18	64	0	r-	Performance Monitor Counter 18
hpmcounter19	64	0	r-	Performance Monitor Counter 19
hpmcounter20	64	0	r-	Performance Monitor Counter 20
hpmcounter21	64	0	r-	Performance Monitor Counter 21
hpmcounter22	64	0	r-	Performance Monitor Counter 22
hpmcounter23	64	0	r-	Performance Monitor Counter 23
hpmcounter24	64	0	r-	Performance Monitor Counter 24
hpmcounter25	64	0	r-	Performance Monitor Counter 25
hpmcounter26	64	0	r-	Performance Monitor Counter 26
hpmcounter27	64	0	r-	Performance Monitor Counter 27
hpmcounter28	64	0	r-	Performance Monitor Counter 28
hpmcounter29	64	0	r-	Performance Monitor Counter 29
hpmcounter30	64	0	r-	Performance Monitor Counter 30
hpmcounter31	64	0	r-	Performance Monitor Counter 31

Table 13.2: Registers at level 2, type:Hart group:User\_Control\_and\_Status

### 13.2.3 Machine\_Control\_and\_Status

Registers at level:2, type:Hart group:Machine\_Control\_and\_Status

Name	Bits	Initial-Hex	RW	Description
mstatus	64	2 00000000	rw	Machine Status
misa	64	80000000 00101107	rw	ISA and Extensions

mie	64	0	rw	Machine Interrupt Enable
mtvec	64	0	rw	Machine Trap-Vector Base-Address
mcounteren	64	0	rw	Machine Counter Enable
mtvt	64	0	rw	Machine CLIC Trap-Vector Base-Address
mcountinhibit	64	0	rw	Machine Counter Inhibit
mhpmevent3	64	0	rw	Machine Performance Monitor Event Select 3
mhpmevent4	64	0	rw	Machine Performance Monitor Event Select 4
mhpmevent5	64	0	rw	Machine Performance Monitor Event Select 5
mhpmevent6	64	0	rw	Machine Performance Monitor Event Select 6
mhpmevent7	64	0	rw	Machine Performance Monitor Event Select 7
mhpmevent8	64	0	rw	Machine Performance Monitor Event Select 8
mhpmevent9	64	0	rw	Machine Performance Monitor Event Select 9
mhpmevent10	64	0	rw	Machine Performance Monitor Event Select 10
mhpmevent11	64	0	rw	Machine Performance Monitor Event Select 11
mhpmevent12	64	0	rw	Machine Performance Monitor Event Select 12
mhpmevent13	64	0	rw	Machine Performance Monitor Event Select 13
mhpmevent14	64	0	rw	Machine Performance Monitor Event Select 14
mhpmevent15	64	0	rw	Machine Performance Monitor Event Select 15
mhpmevent16	64	0	rw	Machine Performance Monitor Event Select 16
mhpmevent17	64	0	rw	Machine Performance Monitor Event Select 17
mhpmevent18	64	0	rw	Machine Performance Monitor Event Select 18
mhpmevent19	64	0	rw	Machine Performance Monitor Event Select 19
mhpmevent20	64	0	rw	Machine Performance Monitor Event Select 20
mhpmevent21	64	0	rw	Machine Performance Monitor Event Select 21
mhpmevent22	64	0	rw	Machine Performance Monitor Event Select 22
mhpmevent23	64	0	rw	Machine Performance Monitor Event Select 23
mhpmevent24	64	0	rw	Machine Performance Monitor Event Select 24
mhpmevent25	64	0	rw	Machine Performance Monitor Event Select 25
mhpmevent26	64	0	rw	Machine Performance Monitor Event Select 26
mhpmevent27	64	0	rw	Machine Performance Monitor Event Select 27
mhpmevent28	64	0	rw	Machine Performance Monitor Event Select 28
mhpmevent29	64	0	rw	Machine Performance Monitor Event Select 29
mhpmevent30	64	0	rw	Machine Performance Monitor Event Select 30
mhpmevent31	64	0	rw	Machine Performance Monitor Event Select 31
mscratch	64	0	rw	Machine Scratch
mepc	64	0	rw	Machine Exception Program Counter
mcause	64	0	rw	Machine Cause
mtval	64	0	rw	Machine Trap Value
mip	64	80	rw	Machine Interrupt Pending
mnxti	64	0	rw	Machine Interrupt Handler Address/Enable
mintstatus	64	0	rw	Machine Interrupt Status
mnscratch	64	0	rw	Machine RNMI Scratch
mnepc	64	0	rw	Machine RNMI Program Counter
mncause	64	0	rw	Machine RNMI Cause
mnstatus	64	8	rw	Machine RNMI Status
pmpcfg0	64	0	rw	Physical Memory Protection Configuration 0
pmpcfg2	64	0	rw	Physical Memory Protection Configuration 2
pmpaddr0	64	0	rw	Physical Memory Protection Address 0
pmpaddr1	64	0	rw	Physical Memory Protection Address 1
pmpaddr2	64	0	rw	Physical Memory Protection Address 2
pmpaddr3	64	0	rw	Physical Memory Protection Address 3
pmpaddr4	64	0	rw	Physical Memory Protection Address 4
pmpaddr5	64	0	rw	Physical Memory Protection Address 5
pmpaddr6	64	0	rw	Physical Memory Protection Address 6
pmpaddr7	64	0	rw	Physical Memory Protection Address 7
pmpaddr8	64	0	rw	Physical Memory Protection Address 8

pmpaddr9	64	0	rw	Physical Memory Protection Address 9
pmpaddr10	64	0	rw	Physical Memory Protection Address 10
pmpaddr11	64	0	rw	Physical Memory Protection Address 11
pmpaddr12	64	0	rw	Physical Memory Protection Address 12
pmpaddr13	64	0	rw	Physical Memory Protection Address 13
pmpaddr14	64	0	rw	Physical Memory Protection Address 14
pmpaddr15	64	0	rw	Physical Memory Protection Address 15
mcycle	64	0	rw	Machine Cycle Counter
minstret	64	0	rw	Machine Instructions Retired
mhpcounter3	64	0	rw	Machine Performance Monitor Counter 3
mhpcounter4	64	0	rw	Machine Performance Monitor Counter 4
mhpcounter5	64	0	rw	Machine Performance Monitor Counter 5
mhpcounter6	64	0	rw	Machine Performance Monitor Counter 6
mhpcounter7	64	0	rw	Machine Performance Monitor Counter 7
mhpcounter8	64	0	rw	Machine Performance Monitor Counter 8
mhpcounter9	64	0	rw	Machine Performance Monitor Counter 9
mhpcounter10	64	0	rw	Machine Performance Monitor Counter 10
mhpcounter11	64	0	rw	Machine Performance Monitor Counter 11
mhpcounter12	64	0	rw	Machine Performance Monitor Counter 12
mhpcounter13	64	0	rw	Machine Performance Monitor Counter 13
mhpcounter14	64	0	rw	Machine Performance Monitor Counter 14
mhpcounter15	64	0	rw	Machine Performance Monitor Counter 15
mhpcounter16	64	0	rw	Machine Performance Monitor Counter 16
mhpcounter17	64	0	rw	Machine Performance Monitor Counter 17
mhpcounter18	64	0	rw	Machine Performance Monitor Counter 18
mhpcounter19	64	0	rw	Machine Performance Monitor Counter 19
mhpcounter20	64	0	rw	Machine Performance Monitor Counter 20
mhpcounter21	64	0	rw	Machine Performance Monitor Counter 21
mhpcounter22	64	0	rw	Machine Performance Monitor Counter 22
mhpcounter23	64	0	rw	Machine Performance Monitor Counter 23
mhpcounter24	64	0	rw	Machine Performance Monitor Counter 24
mhpcounter25	64	0	rw	Machine Performance Monitor Counter 25
mhpcounter26	64	0	rw	Machine Performance Monitor Counter 26
mhpcounter27	64	0	rw	Machine Performance Monitor Counter 27
mhpcounter28	64	0	rw	Machine Performance Monitor Counter 28
mhpcounter29	64	0	rw	Machine Performance Monitor Counter 29
mhpcounter30	64	0	rw	Machine Performance Monitor Counter 30
mhpcounter31	64	0	rw	Machine Performance Monitor Counter 31
mvendorid	64	489	r-	Vendor ID
marchid	64	80000002	r-	Architecture ID
mimpid	64	4210427	r-	Implementation ID
mhartid	64	0	r-	Hardware Thread ID

Table 13.3: Registers at level 2, type:Hart group:Machine\_Control\_and\_Status

### 13.2.4 CLINT

Registers at level:2, type:Hart group:CLINT

Name	Bits	Initial-Hex	RW	Description
msip	8	0	rw	CLINT msip
mtimecmp	64	0	rw	CLINT mtimecmp
mtime	64	0	rw	CLINT mtime

Table 13.4: Registers at level 2, type:Hart group:CLINT

### 13.2.5 Integration\_support

Registers at level:2, type:Hart group:Integration\_support

Name	Bits	Initial-Hex	RW	Description
LRSCAddress	64	ffffff fffffff	rw	LR/SC active lock address
commercial	8	0	r-	Commercial feature in use
ASYNCPE	8	0	r-	Asynchronous Event Pending & Enabled
mask_pmpcfg0	64	ffffff fffffff	r-	Write mask for pmpcfg0
mask_pmpaddr0	64	ffffff fffffff	r-	Write mask for pmpaddr0
mask_pmpaddr1	64	ffffff fffffff	r-	Write mask for pmpaddr1
mask_pmpaddr2	64	ffffff fffffff	r-	Write mask for pmpaddr2
mask_pmpaddr3	64	ffffff fffffff	r-	Write mask for pmpaddr3
mask_pmpaddr4	64	ffffff fffffff	r-	Write mask for pmpaddr4
mask_pmpaddr5	64	ffffff fffffff	r-	Write mask for pmpaddr5
mask_pmpaddr6	64	ffffff fffffff	r-	Write mask for pmpaddr6
mask_pmpaddr7	64	ffffff fffffff	r-	Write mask for pmpaddr7

Table 13.5: Registers at level 2, type:Hart group:Integration\_support