



OVP Guide to Using Processor Models

Model specific information for ARM_ARMv7

Imperas Software Limited
Imperas Buildings, North Weston
Thame, Oxfordshire, OX9 2HA, U.K.
docs@imperas.com



| | |
|----------|--|
| Author | Imperas Software Limited |
| Version | 20200630.0 |
| Filename | OVP_Model_Specific_Information_arm_ARMv7.pdf |
| Created | 2 July 2020 |
| Status | OVP Standard Release |

Copyright Notice

Copyright (c) 2020 Imperas Software Limited. All rights reserved. This software and documentation contain information that is the property of Imperas Software Limited. The software and documentation are furnished under a license agreement and may be used or copied only in accordance with the terms of the license agreement. No part of the software and documentation may be reproduced, transmitted, or translated, in any form or by any means, electronic, mechanical, manual, optical, or otherwise, without prior written permission of Imperas Software Limited, or as expressly provided by the license agreement.

Right to Copy Documentation

The license agreement with Imperas permits licensee to make copies of the documentation for its internal use only. Each copy shall include all copyrights, trademarks, service marks, and proprietary rights notices, if any.

Destination Control Statement

All technical data contained in this publication is subject to the export control laws of the United States of America. Disclosure to nationals of other countries contrary to United States law is prohibited. It is the readers responsibility to determine the applicable regulations and to comply with them.

Disclaimer

IMPERAS SOFTWARE LIMITED, AND ITS LICENSORS MAKE NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

Contents

| | | |
|----------|---|-----------|
| 1 | Overview | 1 |
| 1.1 | Description | 1 |
| 1.2 | Licensing | 1 |
| 1.3 | Limitations | 2 |
| 1.4 | Verification | 2 |
| 1.5 | Features | 3 |
| 1.5.1 | Core Features | 3 |
| 1.5.2 | Memory System | 3 |
| 1.6 | Debug Mask | 3 |
| 1.7 | AArch32 Unpredictable Behavior | 3 |
| 1.7.1 | Equal Target Registers | 3 |
| 1.7.2 | Floating Point Load/Store Multiple Lists | 3 |
| 1.7.3 | Floating Point VLD[2-4]/VST[2-4] Range Overflow | 4 |
| 1.7.4 | If-Then (IT) Block Constraints | 4 |
| 1.7.5 | Use of R13 | 4 |
| 1.7.6 | Use of R15 | 4 |
| 1.7.7 | Unpredictable Instructions in Some Modes | 4 |
| 1.8 | Integration Support | 5 |
| 1.8.1 | Halt Reason Introspection | 5 |
| 1.8.2 | System Register Access Monitor | 5 |
| 1.8.3 | System Register Implementation | 6 |
| 2 | Configuration | 7 |
| 2.1 | Location | 7 |
| 2.2 | GDB Path | 7 |
| 2.3 | Semi-Host Library | 7 |
| 2.4 | Processor Endian-ness | 7 |
| 2.5 | QuantumLeap Support | 7 |
| 2.6 | Processor ELF code | 7 |
| 3 | All Variants in this model | 8 |
| 4 | Bus Master Ports | 11 |
| 5 | Bus Slave Ports | 12 |
| 6 | Net Ports | 13 |

| | | |
|-----------|---|-----------|
| 7 | FIFO Ports | 14 |
| 8 | Formal Parameters | 15 |
| 9 | Execution Modes | 18 |
| 10 | Exceptions | 19 |
| 11 | Hierarchy of the model | 20 |
| 11.1 | Level 1: CPU | 20 |
| 12 | Model Commands | 21 |
| 12.1 | Level 1: CPU | 21 |
| 12.1.1 | debugflags | 21 |
| 12.1.2 | isync | 21 |
| 12.1.3 | itrace | 21 |
| 13 | Registers | 23 |
| 13.1 | Level 1: CPU | 23 |
| 13.1.1 | Core | 23 |
| 13.1.2 | Control | 23 |
| 13.1.3 | User | 23 |
| 13.1.4 | FIQ | 24 |
| 13.1.5 | IRQ | 24 |
| 13.1.6 | Supervisor | 24 |
| 13.1.7 | Monitor | 24 |
| 13.1.8 | Undefined | 25 |
| 13.1.9 | Abort | 25 |
| 13.1.10 | Coprocessor_32_bit | 25 |
| 13.1.11 | Coprocessor_32_bit_secure | 26 |
| 13.1.12 | Coprocessor_32_bit_non_secure | 26 |
| 13.1.13 | Integration_support | 27 |

Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

ARM Processor Model

1.2 Licensing

Usage of binary model under license governing simulator usage.

Note that for models of ARM CPUs the license includes the following terms:

Licensee is granted a non-exclusive, worldwide, non-transferable, revocable licence to:

If no source is being provided to the Licensee: use and copy only (no modifications rights are granted) the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used

to emulate an ARM based system to run application software in a production or live environment.

If source code is being provided to the Licensee: use, copy and modify the model for the sole purpose of designing, developing, analyzing, debugging, testing, verifying, validating and optimizing software which: (a) (i) is for ARM based systems; and (ii) does not incorporate the ARM Models or any part thereof; and (b) such ARM Models may not be used to emulate an ARM based system to run application software in a production or live environment.

In the case of any Licensee who is either or both an academic or educational institution the purposes shall be limited to internal use.

Except to the extent that such activity is permitted by applicable law, Licensee shall not reverse engineer, decompile, or disassemble this model. If this model was provided to Licensee in Europe, Licensee shall not reverse engineer, decompile or disassemble the Model for the purposes of error correction.

The License agreement does not entitle Licensee to manufacture in silicon any product based on this model.

The License agreement does not entitle Licensee to use this model for evaluating the validity of any ARM patent.

Source of model available under separate Imperas Software License Agreement.

1.3 Limitations

Instruction pipelines are not modeled in any way. All instructions are assumed to complete immediately. This means that instruction barrier instructions (e.g. ISB, CP15ISB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. The model does not implement speculative fetch behavior. The branch cache is not modeled.

Caches and write buffers are not modeled in any way. All loads, fetches and stores complete immediately and in order, and are fully synchronous (as if the memory was of Strongly Ordered or Device-nGnRnE type). Data barrier instructions (e.g. DSB, CP15DSB) are treated as NOPs, with the exception of any undefined instruction behavior, which is modeled. Cache manipulation instructions are implemented as NOPs, with the exception of any undefined instruction behavior, which is modeled.

Real-world timing effects are not modeled: all instructions are assumed to complete in a single cycle.

1.4 Verification

Models have been extensively tested by Imperas.

1.5 Features

1.5.1 Core Features

Thumb-2 instructions are supported.

Trivial Jazelle extension is implemented.

1.5.2 Memory System

Security extensions are implemented (also known as TrustZone). Non-secure accesses can be made visible externally by connecting the processor to a 41-bit physical bus, in which case bits 39..0 give the true physical address and bit 40 is the NS bit.

1.6 Debug Mask

It is possible to enable model debug features in various categories. This can be done statically using the “override_debugMask” parameter, or dynamically using the “debugflags” command. Enabled debug features are specified using a bitmask value, as follows:

Value 0x080: enable debugging of all system register accesses.

Value 0x100: enable debugging of all traps of system register accesses.

Value 0x200: enable verbose debugging of other miscellaneous behavior (for example, the reason why a particular instruction is undefined).

All other bits in the debug bitmask are reserved and must not be set to non-zero values.

1.7 AArch32 Unpredictable Behavior

Many AArch32 instruction behaviors are described in the ARM ARM as CONSTRAINED UNPREDICTABLE. This section describes how such situations are handled by this model.

1.7.1 Equal Target Registers

Some instructions allow the specification of two target registers (for example, double-width SMULL, or some VMOV variants), and such instructions are CONSTRAINED UNPREDICTABLE if the same target register is specified in both positions. In this model, such instructions are treated as UNDEFINED.

1.7.2 Floating Point Load/Store Multiple Lists

Instructions that load or store a list of floating point registers (e.g. VSTM, VLDM, VPUSH, VPOP) are CONSTRAINED UNPREDICTABLE if either the uppermost register in the specified

range is greater than 32 or (for 64-bit registers) if more than 16 registers are specified. In this model, such instructions are treated as UNDEFINED.

1.7.3 Floating Point VLD[2-4]/VST[2-4] Range Overflow

Instructions that load or store a fixed number of floating point registers (e.g. VST2, VLD2) are CONSTRAINED UNPREDICTABLE if the upper register bound exceeds the number of implemented floating point registers. In this model, these instructions load and store using modulo 32 indexing (consistent with AArch64 instructions with similar behavior).

1.7.4 If-Then (IT) Block Constraints

Where the behavior of an instruction in an if-then (IT) block is described as CONSTRAINED UNPREDICTABLE, this model treats that instruction as UNDEFINED.

1.7.5 Use of R13

In architecture variants before ARMv8, use of R13 was described as CONSTRAINED UNPREDICTABLE in many circumstances. From ARMv8, most of these situations are no longer considered unpredictable. This model allows R13 to be used like any other GPR, consistent with the ARMv8 specification.

1.7.6 Use of R15

Use of R15 is described as CONSTRAINED UNPREDICTABLE in many circumstances. This model allows such use to be configured using the parameter “unpredictableR15” as follows:

Value “undefined”: any reference to R15 in such a situation is treated as UNDEFINED;

Value “nop”: any reference to R15 in such a situation causes the instruction to be treated as a NOP;

Value “raz_wi”: any reference to R15 in such a situation causes the instruction to be treated as a RAZ/WI (that is, R15 is read as zero and write-ignored);

Value “execute”: any reference to R15 in such a situation is executed using the current value of R15 on read, and writes to R15 are allowed (but are not interworking).

Value “assert”: any reference to R15 in such a situation causes the simulation to halt with an assertion message (allowing any such unpredictable uses to be easily identified).

In this variant, the default value of “unpredictableR15” is “undefined”.

1.7.7 Unpredictable Instructions in Some Modes

Some instructions are described as CONSTRAINED UNPREDICTABLE in some modes only (for example, MSR accessing SPSR is CONSTRAINED UNPREDICTABLE in User and System

modes). This model allows such use to be configured using the parameter “unpredictableModal”, which can have values “undefined” or “nop”. See the previous section for more information about the meaning of these values.

In this variant, the default value of “unpredictableModal” is “nop”.

1.8 Integration Support

This model implements a number of non-architectural pseudo-registers and other features to facilitate integration.

1.8.1 Halt Reason Introspection

An artifact register HaltReason can be read to determine the reason or reasons that a processor is halted. This register is a bitfield, with the following encoding: bit 0 indicates the processor has executed a wait-for-event (WFE) instruction; bit 1 indicates the processor has executed a wait-for-interrupt (WFI) instruction; and bit 2 indicates the processor is held in reset.

1.8.2 System Register Access Monitor

If parameter “enableSystemMonitorBus” is True, an artifact 32-bit bus “SystemMonitor” is enabled for each PE. Every system register read or write by that PE is then visible as a read or write on this artifact bus, and can therefore be monitored using callbacks installed in the client environment (use opBusReadMonitorAdd/opBusWriteMonitorAdd or icmAddBusReadCallback/icmAddBusWriteCallback, depending on the client API). The format of the address on the bus is as follows:

bits 31:26 - zero

bit 25 - 1 if AArch64 access, 0 if AArch32 access

bit 24 - 1 if non-secure access, 0 if secure access

bits 23:20 - CRm value

bits 19:16 - CRn value

bits 15:12 - op2 value

bits 11:8 - op1 value

bits 7:4 - op0 value (AArch64) or coprocessor number (AArch32)

bits 3:0 - zero

As an example, to view non-secure writes to writes to CNTFRQ_EL0 in AArch64 state, install a write monitor on address range 0x020e0330:0x020e0333.

1.8.3 System Register Implementation

If parameter “enableSystemBus” is True, an artifact 32-bit bus “System” is enabled for each PE. Slave callbacks installed on this bus can be used to implement modified system register behavior (use opBusSlaveNew or icmMapExternalMemory, depending on the client API). The format of the address on the bus is the same as for the system monitor bus, described above.

Chapter 2

Configuration

2.1 Location

This model's VLVN is arm.ovpworld.org/processor/arm/1.0.

The model source is usually at:

`$IMPERAS_HOME/ImperasLib/source/arm.ovpworld.org/processor/arm/1.0`

The model binary is usually at:

`$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/arm.ovpworld.org/processor/arm/1.0`

2.2 GDB Path

The default GDB for this model is: `$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/arm-none-eabi-gdb`.

2.3 Semi-Host Library

The default semi-host library file is `arm.ovpworld.org/semihosting/armNewlib/1.0`

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: `0x28`.

Chapter 3

All Variants in this model

This model has these variants

| Variant | Description |
|----------------|------------------------------|
| ARMv4T | |
| ARMv4xM | |
| ARMv4 | |
| ARMv4TxM | |
| ARMv5xM | |
| ARMv5 | |
| ARMv5TxM | |
| ARMv5T | |
| ARMv5TExP | |
| ARMv5TE | |
| ARMv5TEJ | |
| ARMv6 | |
| ARMv6K | |
| ARMv6T2 | |
| ARMv6KZ | |
| ARMv7 | (described in this document) |
| ARM7TDMI | |
| ARM7EJ-S | |
| ARM720T | |
| ARM920T | |
| ARM922T | |
| ARM926EJ-S | |
| ARM940T | |
| ARM946E | |
| ARM966E | |
| ARM968E-S | |
| ARM1020E | |
| ARM1022E | |
| ARM1026EJ-S | |
| ARM1136J-S | |
| ARM1156T2-S | |

| | |
|----------------|--|
| ARM1176JZ-S | |
| Cortex-R4 | |
| Cortex-R4F | |
| Cortex-A5UP | |
| Cortex-A5MPx1 | |
| Cortex-A5MPx2 | |
| Cortex-A5MPx3 | |
| Cortex-A5MPx4 | |
| Cortex-A8 | |
| Cortex-A9UP | |
| Cortex-A9MPx1 | |
| Cortex-A9MPx2 | |
| Cortex-A9MPx3 | |
| Cortex-A9MPx4 | |
| Cortex-A7UP | |
| Cortex-A7MPx1 | |
| Cortex-A7MPx2 | |
| Cortex-A7MPx3 | |
| Cortex-A7MPx4 | |
| Cortex-A15UP | |
| Cortex-A15MPx1 | |
| Cortex-A15MPx2 | |
| Cortex-A15MPx3 | |
| Cortex-A15MPx4 | |
| Cortex-A17MPx1 | |
| Cortex-A17MPx2 | |
| Cortex-A17MPx3 | |
| Cortex-A17MPx4 | |
| AArch32 | |
| AArch64 | |
| Cortex-A32MPx1 | |
| Cortex-A32MPx2 | |
| Cortex-A32MPx3 | |
| Cortex-A32MPx4 | |
| Cortex-A35MPx1 | |
| Cortex-A35MPx2 | |
| Cortex-A35MPx3 | |
| Cortex-A35MPx4 | |
| Cortex-A53MPx1 | |
| Cortex-A53MPx2 | |
| Cortex-A53MPx3 | |
| Cortex-A53MPx4 | |
| Cortex-A55MPx1 | |
| Cortex-A55MPx2 | |
| Cortex-A55MPx3 | |

| | |
|----------------|--|
| Cortex-A55MPx4 | |
| Cortex-A57MPx1 | |
| Cortex-A57MPx2 | |
| Cortex-A57MPx3 | |
| Cortex-A57MPx4 | |
| Cortex-A72MPx1 | |
| Cortex-A72MPx2 | |
| Cortex-A72MPx3 | |
| Cortex-A72MPx4 | |
| Cortex-A73MPx1 | |
| Cortex-A73MPx2 | |
| Cortex-A73MPx3 | |
| Cortex-A73MPx4 | |
| Cortex-A75MPx1 | |
| Cortex-A75MPx2 | |
| Cortex-A75MPx3 | |
| Cortex-A75MPx4 | |
| MultiCluster | |

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

| Name | min | max | Connect? | Description |
|-------------|-----|-----|-----------|-------------|
| INSTRUCTION | 32 | 41 | mandatory | |
| DATA | 32 | 41 | optional | |

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

| Name | Type | Connect? | Description |
|--------------|-------|----------|--|
| reset | input | optional | Processor reset, active high |
| fiq | input | optional | FIQ interrupt, active high (negation of nFIQ) |
| irq | input | optional | IRQ interrupt, active high (negation of nIRQ) |
| sei | input | optional | System error interrupt, active on rising edge (negation of nSEI) |
| AXI_SLVERR | input | optional | AXI external abort type (DECERR=0, SLVERR=1) |
| CP15SDISABLE | input | optional | CP15SDISABLE (active high) |

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

| Name | Type | Description |
|--------------------------|-------------|---|
| variant | Enumeration | Selects variant (either a generic ISA or a specific model) |
| verbose | Boolean | Specify verbosity of output |
| suppressCPSWarnings | Boolean | Suppress duplicate warnings generated using ARM_CP_CPSI or ARM_CP_CPSD message identifiers |
| showHiddenRegs | Boolean | Show hidden registers during register tracing |
| UAL | Boolean | Disassemble using UAL syntax |
| enableVFPAtReset | Boolean | Enable vector floating point (SIMD and VFP) instructions at reset. (Enables cp10/11 in CPACR and sets FPEXC.EN) |
| enableSystemBus | Boolean | Add 32-bit artifact System bus port, allowing system registers to be externally implemented |
| enableSystemMonitorBus | Boolean | Add 32-bit artifact SystemMonitor bus port, allowing system register accesses to be externally monitored |
| compatibility | Enumeration | Specify compatibility mode (ISA, gdb or nopSVC) |
| unpredictableR15 | Enumeration | Specify behavior for UNPREDICTABLE uses of AArch32 R15 register (undefined, nop, raz_wi, execute or assert) |
| unpredictableModal | Enumeration | Specify behavior for UNPREDICTABLE instructions in certain AArch32 modes (for example, MRS using SPSR in System mode) (undefined, nop or assert) |
| maxSIMDUnroll | Uns32 | If SIMD operations are supported, specify the maximum number of parallel SIMD operations to unroll (unrolled operations can be faster, but produce more verbose JIT code) |
| override_debugMask | Uns32 | Specifies debug mask, enabling debug output for model components |
| endian | Endian | Model endian |
| override_fcsePresent | Boolean | Specifies that FCSE is present (if true) |
| override_fpexcDexPresent | Boolean | Specifies that the FPEXC.DEX register field is implemented (if true) |
| override_advSIMDPresent | Boolean | Specifies that Advanced SIMD extensions are present (if true) |
| override_vfpPresent | Boolean | Specifies that VFP extensions are present (if true) |
| override_physicalBits | Uns32 | Specifies the implemented physical bus bits (defaults to connected physical bus width) |
| override_SCTLR_V | Boolean | Override SCTLR.V with the passed value (enables high vectors; also configurable using VINITHI pin) |
| override_SCTLR_IE | Boolean | Override SCTLR.IE with the passed value (configures instruction endianness; also configurable using CFGIE pin) |

| | | |
|---------------------------------|---------|--|
| override_SCTLR_EE | Boolean | Override SCTLR.EE with the passed value (configures exception data endianness; also configurable using CFGEE pin) |
| override_SCTLR_TE | Boolean | Override SCTLR.TE with the passed value (configures Thumb state for exception handling; also configurable using TEINIT pin) |
| override_SCTLR_NMFI | Boolean | Override SCTLR.NMFI with the passed value (configures NMFI state for exception handling; also configurable using CFGNMFI pin) |
| override_SCTLR_CP15BEN_Present | Boolean | Enable ARMv7 SCTLR.CP15BEN bit (CP15 barrier enable) |
| override_MIDR | Uns32 | Override MIDR/MIDR_EL1 register |
| override_CTR | Uns32 | Override CTR/CTR_EL0 register |
| override_CLIDR | Uns32 | Override CLIDR/CLIDR_EL1 register |
| override_AIDR | Uns32 | Override AIDR/AIDR_EL1 register |
| override_PFR0 | Uns32 | Override ID_PFR0/ID_PFR0_EL1 register |
| override_PFR1 | Uns32 | Override ID_PFR1/ID_PFR1_EL1 register |
| override_DFR0 | Uns32 | Override ID_DFR0/ID_DFR0_EL1 register |
| override_AFR0 | Uns32 | Override ID_AFR0/ID_AFR0_EL1 register |
| override_MMFR0 | Uns32 | Override ID_MMFR0/ID_MMFR0_EL1 register |
| override_MMFR1 | Uns32 | Override ID_MMFR1/ID_MMFR1_EL1 register |
| override_MMFR2 | Uns32 | Override ID_MMFR2/ID_MMFR2_EL1 register |
| override_MMFR3 | Uns32 | Override ID_MMFR3/ID_MMFR3_EL1 register |
| override_ISAR0 | Uns32 | Override ID_ISAR0/ID_ISAR0_EL1 register |
| override_ISAR1 | Uns32 | Override ID_ISAR1/ID_ISAR1_EL1 register |
| override_ISAR2 | Uns32 | Override ID_ISAR2/ID_ISAR2_EL1 register |
| override_ISAR3 | Uns32 | Override ID_ISAR3/ID_ISAR3_EL1 register |
| override_ISAR4 | Uns32 | Override ID_ISAR4/ID_ISAR4_EL1 register |
| override_ISAR5 | Uns32 | Override ID_ISAR5/ID_ISAR5_EL1 register |
| override_DBGDIDR | Uns32 | Override DBGDIDR register (not functionally significant in the model) |
| override_FPSID | Uns32 | Override SIMD/VFP FPSID register |
| override_MVFR0 | Uns32 | Override SIMD/VFP MVFR0/MVFR0_EL1 register |
| override_MVFR1 | Uns32 | Override SIMD/VFP MVFR1/MVFR1_EL1 register |
| override_FPEXC | Uns32 | Override SIMD/VFP FPEXC/FPEXC32_EL2 register |
| override_ERG | Uns32 | Specifies exclusive reservation granule |
| override_STRoffsetPC12 | Boolean | Specifies that STR/STR of PC should do so with 12:byte offset from the current instruction (if true), otherwise an 8:byte offset is used |
| override_ignoreBadCp15 | Boolean | Specifies whether invalid coprocessor 15 access should be ignored (if true) or cause Invalid Instruction exceptions (if false) |
| override_SGIDisable | Boolean | Override whether GIC SGIs may be disabled (if true) or are permanently enabled (if false) |
| override_condUndefined | Boolean | Force undefined instructions to take Undefined Instruction exception even if they are conditional |
| override_deviceStrongAligned | Boolean | Force accesses to Device and Strongly Ordered regions to be aligned |
| override_Control_V | Boolean | Override SCTLR.V with the passed value (deprecated, use override_SCTLR_V) |
| override_MainId | Uns32 | Override MIDR register (deprecated, use override_MIDR) |
| override_CacheType | Uns32 | Override CTR register (deprecated, use override_CTR) |
| override_InstructionAttributes0 | Uns32 | Override ID_ISAR0 register (deprecated, use override_ISAR0) |
| override_InstructionAttributes1 | Uns32 | Override ID_ISAR1 register (deprecated, use override_ISAR1) |

| | | |
|---------------------------------|-------|---|
| override.InstructionAttributes2 | Uns32 | Override ID_ISAR2 register (deprecated, use override_ISAR2) |
| override.InstructionAttributes3 | Uns32 | Override ID_ISAR3 register (deprecated, use override_ISAR3) |
| override.InstructionAttributes4 | Uns32 | Override ID_ISAR4 register (deprecated, use override_ISAR4) |
| override.InstructionAttributes5 | Uns32 | Override ID_ISAR5 register (deprecated, use override_ISAR5) |

Table 8.1: Parameters that can be set in: CPU

Chapter 9

Execution Modes

| Mode | Code |
|------------|------|
| User | 16 |
| FIQ | 17 |
| IRQ | 18 |
| Supervisor | 19 |
| Monitor | 22 |
| Abort | 23 |
| Undefined | 27 |
| System | 31 |

Table 9.1: Modes implemented in: CPU

Chapter 10

Exceptions

| Exception | Code |
|-------------------|------|
| Reset | 0 |
| Undefined | 1 |
| SupervisorCall | 2 |
| SecureMonitorCall | 3 |
| PrefetchAbort | 5 |
| DataAbort | 6 |
| IRQ | 8 |
| FIQ | 9 |

Table 10.1: Exceptions implemented in: CPU

Chapter 11

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1: CPU

This level in the model hierarchy has 3 commands.

This level in the model hierarchy has 13 register groups:

| Group name | Registers |
|-------------------------------|-----------|
| Core | 16 |
| Control | 3 |
| User | 7 |
| FIQ | 8 |
| IRQ | 3 |
| Supervisor | 3 |
| Monitor | 3 |
| Undefined | 3 |
| Abort | 3 |
| Coprocessor_32_bit | 53 |
| Coprocessor_32_bit_secure | 6 |
| Coprocessor_32_bit_non_secure | 6 |
| Integration_support | 3 |

Table 11.1: Register groups

This level in the model hierarchy has no children.

Chapter 12

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1: CPU

12.1.1 debugflags

show or modify the processor debug flags

| Argument | Type | Description |
|----------|---------|---|
| -get | Boolean | print current processor flags value |
| -mask | Boolean | print valid debug flag bits |
| -set | Int32 | new processor flags (only flags 0x000003e4 can be modified) |

Table 12.1: debugflags command arguments

12.1.2 isync

specify instruction address range for synchronous execution

| Argument | Type | Description |
|------------|-------|--|
| -addresshi | Uns64 | end address of synchronous execution range |
| -addresslo | Uns64 | start address of synchronous execution range |

Table 12.2: isync command arguments

12.1.3 itrace

enable or disable instruction tracing

| Argument | Type | Description |
|-------------------|---------|--|
| -after | Uns64 | apply after this many instructions |
| -enable | Boolean | enable instruction tracing |
| -instructioncount | Boolean | include the instruction number in each trace |
| -off | Boolean | disable instruction tracing |

| | | |
|-----------------|---------|--|
| -on | Boolean | enable instruction tracing |
| -registerchange | Boolean | show registers changed by this instruction |
| -registers | Boolean | show registers after each trace |

Table 12.3: itrace command arguments

Chapter 13

Registers

13.1 Level 1: CPU

13.1.1 Core

Registers at level:1, type:CPU group:Core

| Name | Bits | Initial-Hex | RW | Description |
|------|------|-------------|----|-----------------|
| r0 | 32 | 0 | rw | |
| r1 | 32 | 0 | rw | |
| r2 | 32 | 0 | rw | |
| r3 | 32 | 0 | rw | |
| r4 | 32 | 0 | rw | |
| r5 | 32 | 0 | rw | |
| r6 | 32 | 0 | rw | |
| r7 | 32 | 0 | rw | |
| r8 | 32 | 0 | rw | |
| r9 | 32 | 0 | rw | |
| r10 | 32 | 0 | rw | |
| r11 | 32 | 0 | rw | frame pointer |
| r12 | 32 | 0 | rw | |
| sp | 32 | 0 | rw | stack pointer |
| lr | 32 | 0 | rw | |
| pc | 32 | 0 | rw | program counter |

Table 13.1: Registers at level 1, type:CPU group:Core

13.1.2 Control

Registers at level:1, type:CPU group:Control

| Name | Bits | Initial-Hex | RW | Description |
|------|------|-------------|----|------------------------------|
| fps | 32 | 0 | rw | archaic FPSCR view (for gdb) |
| cpsr | 32 | 1d3 | rw | |
| spsr | 32 | 0 | rw | |

Table 13.2: Registers at level 1, type:CPU group:Control

13.1.3 User

Registers at level:1, type:CPU group:User

| Name | Bits | Initial-Hex | RW | Description |
|---------|------|-------------|----|-------------|
| r8_usr | 32 | 0 | rw | |
| r9_usr | 32 | 0 | rw | |
| r10_usr | 32 | 0 | rw | |
| r11_usr | 32 | 0 | rw | |
| r12_usr | 32 | 0 | rw | |
| sp_usr | 32 | 0 | rw | |
| lr_usr | 32 | 0 | rw | |

Table 13.3: Registers at level 1, type:CPU group:User

13.1.4 FIQ

Registers at level:1, type:CPU group:FIQ

| Name | Bits | Initial-Hex | RW | Description |
|----------|------|-------------|----|-------------|
| r8_fiq | 32 | 0 | rw | |
| r9_fiq | 32 | 0 | rw | |
| r10_fiq | 32 | 0 | rw | |
| r11_fiq | 32 | 0 | rw | |
| r12_fiq | 32 | 0 | rw | |
| sp_fiq | 32 | 0 | rw | |
| lr_fiq | 32 | 0 | rw | |
| spsr_fiq | 32 | 0 | rw | |

Table 13.4: Registers at level 1, type:CPU group:FIQ

13.1.5 IRQ

Registers at level:1, type:CPU group:IRQ

| Name | Bits | Initial-Hex | RW | Description |
|----------|------|-------------|----|-------------|
| sp_irq | 32 | 0 | rw | |
| lr_irq | 32 | 0 | rw | |
| spsr_irq | 32 | 0 | rw | |

Table 13.5: Registers at level 1, type:CPU group:IRQ

13.1.6 Supervisor

Registers at level:1, type:CPU group:Supervisor

| Name | Bits | Initial-Hex | RW | Description |
|----------|------|-------------|----|-------------|
| sp_svc | 32 | 0 | rw | |
| lr_svc | 32 | 0 | rw | |
| spsr_svc | 32 | 0 | rw | |

Table 13.6: Registers at level 1, type:CPU group:Supervisor

13.1.7 Monitor

Registers at level:1, type:CPU group:Monitor

| Name | Bits | Initial-Hex | RW | Description |
|--------|------|-------------|----|-------------|
| sp_mon | 32 | 0 | rw | |

| | | | | |
|----------|----|---|----|--|
| lr_mon | 32 | 0 | rw | |
| spsr_mon | 32 | 0 | rw | |

Table 13.7: Registers at level 1, type:CPU group:Monitor

13.1.8 Undefined

Registers at level:1, type:CPU group:Undefined

| Name | Bits | Initial-Hex | RW | Description |
|------------|------|-------------|----|-------------|
| sp_undef | 32 | 0 | rw | |
| lr_undef | 32 | 0 | rw | |
| spsr_undef | 32 | 0 | rw | |

Table 13.8: Registers at level 1, type:CPU group:Undefined

13.1.9 Abort

Registers at level:1, type:CPU group:Abort

| Name | Bits | Initial-Hex | RW | Description |
|----------|------|-------------|----|-------------|
| sp_abt | 32 | 0 | rw | |
| lr_abt | 32 | 0 | rw | |
| spsr_abt | 32 | 0 | rw | |

Table 13.9: Registers at level 1, type:CPU group:Abort

13.1.10 Coprocessor_32_bit

Registers at level:1, type:CPU group:Coprocessor_32_bit

| Name | Bits | Initial-Hex | RW | Description |
|------------|------|-------------|----|---|
| ADFSR | 32 | 0 | rw | Auxiliary Data Fault Status |
| AIFSR | 32 | 0 | rw | Auxiliary Instruction Fault Status |
| ATS12NSOPR | 32 | - | -w | Address Translate Stages 1 and 2 Non-Secure Only EL1 Read |
| ATS12NSOPW | 32 | - | -w | Address Translate Stages 1 and 2 Non-Secure Only EL1 Write |
| ATS12NSOUR | 32 | - | -w | Address Translate Stages 1 and 2 Non-Secure Only Unprivileged Read |
| ATS12NSOUW | 32 | - | -w | Address Translate Stages 1 and 2 Non-Secure Only Unprivileged Write |
| BPIALL | 32 | - | -w | Branch Predictor Invalidate All |
| BPIMVA | 32 | - | -w | Branch Predictor Invalidate by VA |
| CCSIDR | 32 | 0 | r- | Cache Size ID |
| CLIDR | 32 | 0 | r- | Cache Level ID |
| CP15NOP | 32 | - | -w | CP15 NOP |
| CPACR | 32 | 0 | rw | Coprocessor Access Control |
| CSSELR | 32 | 0 | rw | Cache Size Selection |
| DBGDIDR | 32 | 0 | r- | Debug ID |
| DCCIMVAC | 32 | - | -w | Data Cache Line Clean and Invalidate by VA to PoC |
| DCCISW | 32 | - | -w | Data Cache Line Clean and Invalidate by Set/Way |
| DCCMVAC | 32 | - | -w | Data Cache Line Clean by VA to PoC |
| DCCMVAU | 32 | - | -w | Data Cache Line Clean by VA to PoU |
| DCCSW | 32 | - | -w | Data Cache Line Clean by Set/Way |
| DCIMVAC | 32 | - | -w | Data Cache Line Invalidate by VA to PoC |
| DCISW | 32 | - | -w | Data Cache Line Invalidate by Set/Way |

| | | | | |
|----------|----|---|----|------------------------------------|
| ICIALLU | 32 | - | -w | Instruction Cache Invalidate All |
| ICIMVAU | 32 | - | -w | Instruction Cache Invalidate by VA |
| ID_AFR0 | 32 | 0 | r- | Auxiliary Feature 0 |
| ID_DFR0 | 32 | 0 | r- | Debug Feature 0 |
| ID_ISAR0 | 32 | 0 | r- | Instruction Set Attribute 0 |
| ID_ISAR1 | 32 | 0 | r- | Instruction Set Attribute 1 |
| ID_ISAR2 | 32 | 0 | r- | Instruction Set Attribute 2 |
| ID_ISAR3 | 32 | 0 | r- | Instruction Set Attribute 3 |
| ID_ISAR4 | 32 | 0 | r- | Instruction Set Attribute 4 |
| ID_ISAR5 | 32 | 0 | r- | Instruction Set Attribute 5 |
| ID_MMFR0 | 32 | 0 | r- | Memory Model Feature 0 |
| ID_MMFR1 | 32 | 0 | r- | Memory Model Feature 1 |
| ID_MMFR2 | 32 | 0 | r- | Memory Model Feature 2 |
| ID_MMFR3 | 32 | 0 | r- | Memory Model Feature 3 |
| ID_PFR0 | 32 | 0 | r- | Processor Feature 0 |
| ID_PFR1 | 32 | 0 | r- | Processor Feature 1 |
| ISR | 32 | 0 | r- | Interrupt Status |
| JIDR | 32 | 0 | rw | Jazelle ID |
| JMCR | 32 | 0 | rw | Jazelle Main Configuration |
| JOSCR | 32 | 0 | rw | Jazelle OS Control |
| MIDR | 32 | 0 | r- | Main ID |
| MPIDR | 32 | 0 | r- | Multiprocessor Affinity |
| MVBAR | 32 | 0 | rw | Monitor Vector Base Address |
| NSACR | 32 | 0 | rw | Non-Secure Access Control |
| PAR | 32 | 0 | rw | Physical Address |
| SCR | 32 | 0 | rw | Secure Configuration |
| SCTLR | 32 | 0 | rw | System Control |
| SDER | 32 | 0 | rw | Secure Debug Enable |
| TCMTR | 32 | 0 | r- | TCM Type |
| TEECR | 32 | 0 | rw | T32EE Configuration |
| TEEHBR | 32 | 0 | rw | T32EE Handler Base |
| VBAR | 32 | 0 | rw | Vector Base Address |

Table 13.10: Registers at level 1, type:CPU group:Coprocessor_32_bit

13.1.11 Coprocessor_32_bit_secure

Registers at level:1, type:CPU group:Coprocessor_32_bit_secure

| Name | Bits | Initial-Hex | RW | Description |
|----------|------|-------------|----|------------------------------------|
| ADFSR_S | 32 | 0 | rw | Auxiliary Data Fault Status |
| AIFSR_S | 32 | 0 | rw | Auxiliary Instruction Fault Status |
| CSSELR_S | 32 | 0 | rw | Cache Size Selection |
| PAR_S | 32 | 0 | rw | Physical Address |
| SCTLR_S | 32 | 0 | rw | System Control |
| VBAR_S | 32 | 0 | rw | Vector Base Address |

Table 13.11: Registers at level 1, type:CPU group:Coprocessor_32_bit_secure

13.1.12 Coprocessor_32_bit_non_secure

Registers at level:1, type:CPU group:Coprocessor_32_bit_non_secure

| Name | Bits | Initial-Hex | RW | Description |
|----------|------|-------------|----|-----------------------------|
| ADFSR_NS | 32 | 0 | rw | Auxiliary Data Fault Status |

| | | | | |
|-----------|----|---|----|------------------------------------|
| AIFSR_NS | 32 | 0 | rw | Auxiliary Instruction Fault Status |
| CSSELR_NS | 32 | 0 | rw | Cache Size Selection |
| PAR_NS | 32 | 0 | rw | Physical Address |
| SCTLR_NS | 32 | 0 | rw | System Control |
| VBAR_NS | 32 | 0 | rw | Vector Base Address |

Table 13.12: Registers at level 1, type:CPU group:Coprocessor_32_bit_non_secure

13.1.13 Integration_support

Registers at level:1, type:CPU group:Integration_support

| Name | Bits | Initial-Hex | RW | Description |
|------------|------|-------------|----|---|
| transactPL | 32 | 1 | r- | privilege level of current memory transaction |
| transactAT | 32 | 0 | r- | current memory transaction type: PA=1, VA=0 |
| HaltReason | 8 | 0 | r- | bit field indicating halt reason |

Table 13.13: Registers at level 1, type:CPU group:Integration_support