



OVP Guide to Using Processor Models

Model specific information for MIPS_M5150

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| Author | Imperas Software Limited |
| Version | 20210408.0 |
| Filename | OVP_Model_Specific_Information_mips32_M5150.pdf |
| Created | 9 April 2021 |
| Status | OVP Standard Release |

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Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit OVPworld.org.

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Chapter 1

Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

1.1 Description

MIPS32 Configurable Processor Model

If you need other variants, these models can be obtained from www.OVPworld.org/MIPUser.

1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

1.3 Limitations

If this model is not part of your installation, then it is available for download from www.OVPworld.org/MIPUser.

1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

1.5 Features

Both MIPS32 and microMIPS32 Instruction sets implemented. MIPS32 used when coming out of reset

MMU Type: Standard TLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MCU ASE implemented

DSP ASE Rev 2 implemented

Chapter 2

Configuration

2.1 Location

This model's VLN is `mips.ovpworld.org/processor/mips32/1.0`.

The model source is usually at:

`$IMPERAS_HOME/ImperasLib/source/mips.ovpworld.org/processor/mips32/1.0`

The model binary is usually at:

`$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/mips.ovpworld.org/processor/mips32/1.0`

2.2 GDB Path

The default GDB for this model is: `$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/mips-sde-elf-gdb`.

2.3 Semi-Host Library

The default semi-host library file is `mips.ovpworld.org/semihosting/mips32Newlib/1.0`

2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

2.6 Processor ELF code

The ELF code supported by this model is: `0x8`.

Chapter 3

All Variants in this model

This model has these variants

| Variant | Description |
|----------------|------------------------------|
| I7200 | |
| M5100 | |
| M5150 | (described in this document) |
| M6200 | |
| M6250 | |
| MIPS32R6 | |
| P5600 | |

Table 3.1: All Variants in this model

Chapter 4

Bus Master Ports

This model has these bus master ports.

| Name | min | max | Connect? | Description |
|-------------|-----|-----|-----------|----------------------------|
| ISPRAM | 32 | 32 | optional | instruction scratchpad RAM |
| DSPRAM | 32 | 32 | optional | data scratchpad RAM |
| INSTRUCTION | 12 | 36 | mandatory | |
| DATA | 12 | 36 | optional | |

Table 4.1: Bus Master Ports

Chapter 5

Bus Slave Ports

This model has no bus slave ports.

Chapter 6

Net Ports

This model has these net ports.

| Name | Type | Connect? | Description |
|---------------------|--------|----------|---|
| reset | input | optional | Core reset |
| softreset | input | optional | Core soft reset |
| dint | input | optional | Debug external interrupt |
| hwint0 | input | optional | External interrupt |
| hwint1 | input | optional | External interrupt |
| hwint2 | input | optional | External interrupt |
| hwint3 | input | optional | External interrupt |
| hwint4 | input | optional | External interrupt |
| hwint5 | input | optional | External interrupt |
| hwint6 | input | optional | External interrupt |
| hwint7 | input | optional | External interrupt |
| nmi | input | optional | Non-maskable external interrupt |
| EICPresent | input | optional | Input signal SLEICPresent per VPE |
| EIC_RIPL | input | optional | External interrupt controller RIPL (alias of hwint0 - 5 or 7) |
| EIC_EICSS | input | optional | External interrupt controller EICSS |
| EIC_VectorNum | input | optional | External interrupt controller vector number |
| EIC_VectorOffset | input | optional | External interrupt controller vector offset |
| EIC_GID | input | optional | External interrupt controller guest ID |
| intISS | output | optional | True when interrupt request is serviced |
| causeTI | output | optional | True when timer interrupt expires |
| causeIP0 | output | optional | Raised for software interrupt request IP0 |
| causeIP1 | output | optional | Raised for software interrupt request IP1 |
| si_sleep | output | optional | True when the VPE is in WAIT state |
| vc_run | input | optional | Set to force stop of execution on processor VPE (simulation control only) |
| Guest.EIC_RIPL | input | optional | Guest External interrupt controller RIPL |
| Guest.EIC_EICSS | input | optional | Guest External interrupt controller EICSS |
| Guest.EIC_VectorNum | input | optional | Guest External interrupt controller vector number |

| | | | |
|------------------------|--------|----------|---|
| Guest.EIC_VectorOffset | input | optional | Guest External interrupt controller vector offset |
| Guest.EIC_GID | input | optional | Guest External interrupt controller guest ID |
| Guest.intISS | output | optional | True when Guest interrupt request is serviced |
| Guest.causeTI | output | optional | True when Guest timer interrupt expires |
| Guest.causeIP0 | output | optional | Raised for Guest software interrupt request IP0 |
| Guest.causeIP1 | output | optional | Raised for Guest software interrupt request IP1 |

Table 6.1: Net Ports

Chapter 7

FIFO Ports

This model has no FIFO ports.

Chapter 8

Formal Parameters

| Name | Type | Description |
|--------------------------|-------------|--|
| variant | Enumeration | Processor variant |
| endian | Endian | Model endian |
| cacheenable | Enumeration | Select cache model mode (default, tag or full) |
| cachedebug | Uns32 | Cache debug flags |
| cacheextbiuinfo | Pointer | Pointer to platform-provided BIU cache info structure |
| mipsHexFile | String | Load a MIPS hex file (test-mode) |
| IMPERAS_MIPS_AVP_OPCODES | Boolean | Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination) |
| cacheIndexBypassTLB | Boolean | When set, cache index ops do not generate TLB exceptions |
| MIPS_TRACE | Boolean | Enable MIPS-format trace output |
| gprNames | Boolean | Disassemble the register names from the default ABI instead of register numbers for MIPS-format trace output |
| supervisorMode | Boolean | Override whether processor implements supervisor mode |
| busErrors | Boolean | Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions |
| fixedMMU | Boolean | Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0) |
| fixedDbgRegSize | Boolean | Enable applications to debug on P5600 with GDB version 2015.06-05 and prior |
| removeDSP | Boolean | Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0) |
| removeCMP | Boolean | Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0) |
| removeFP | Boolean | Override the FP-Present configuration when true (sets Config1.FP to 0) |
| removeFTLB | Boolean | Override the FTLBEn configuration when true (disable FTLB) |
| isISA | Boolean | Enable to specify ISA model (reset address from ELF, all coprocessors enabled) |
| hiddenTLBentries | Boolean | Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance |
| perfCounters | Uns32 | Performance Counters |
| MTFPU | Uns32 | Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior) |
| supportDenormals | Boolean | Enable to specify that the FPU supports denormal operands and results |
| VPE0MaxTC | Uns32 | Specifies the maximum TCs initially on VPE0. Ignored if less than two VPEs configured. |

| | | |
|----------------------|---------|--|
| VPE1MaxTC | Uns32 | Specifies the maximum TCs initially on VPE1. Ignored if less than three VPEs configured. |
| mpuRegions | Uns32 | Number of regions for memory protection unit |
| mpuType | Uns32 | Type of MPU implementation |
| mpuEnable | Boolean | Enable MPU2 segment control at reset |
| mpuSegment0 | Uns32 | Attributes for segment 0 in MPU2 SegmentControl_0 register |
| mpuSegment1 | Uns32 | Attributes for segment 1 in MPU2 SegmentControl_0 register |
| mpuSegment2 | Uns32 | Attributes for segment 2 in MPU2 SegmentControl_0 register |
| mpuSegment3 | Uns32 | Attributes for segment 3 in MPU2 SegmentControl_0 register |
| mpuSegment4 | Uns32 | Attributes for segment 4 in MPU2 SegmentControl_1 register |
| mpuSegment5 | Uns32 | Attributes for segment 5 in MPU2 SegmentControl_1 register |
| mpuSegment6 | Uns32 | Attributes for segment 6 in MPU2 SegmentControl_1 register |
| mpuSegment7 | Uns32 | Attributes for segment 7 in MPU2 SegmentControl_1 register |
| mpuSegment8 | Uns32 | Attributes for segment 8 in MPU2 SegmentControl_2 register |
| mpuSegment9 | Uns32 | Attributes for segment 9 in MPU2 SegmentControl_2 register |
| mpuSegment10 | Uns32 | Attributes for segment 10 in MPU2 SegmentControl_2 register |
| mpuSegment11 | Uns32 | Attributes for segment 11 in MPU2 SegmentControl_2 register |
| mpuSegment12 | Uns32 | Attributes for segment 12 in MPU2 SegmentControl_3 register |
| mpuSegment13 | Uns32 | Attributes for segment 13 in MPU2 SegmentControl_3 register |
| mpuSegment14 | Uns32 | Attributes for segment 14 in MPU2 SegmentControl_3 register |
| mpuSegment15 | Uns32 | Attributes for segment 15 in MPU2 SegmentControl_3 register |
| mvpconf0vpe | Uns32 | Override MVPConf0.PVPE |
| tcDisable | Uns32 | Number of disabled TCs |
| vpeDisable | Uns32 | Number of disabled VPEs |
| mvpconf0tc | Uns32 | Override MVPConf0.PTC |
| mvpconf0pcp | Boolean | Override MVPConf0.PCP |
| mvpconf0tcp | Boolean | Override MVPConf0.TCP |
| mvpconf0c1f | Boolean | Override MVPConf.C1F |
| mvpcontrolPolicyMode | Boolean | Override MVPControl.POLICY_MODE |
| hasFDC | Uns32 | Specify the size of Fast Debug Channel register block |
| licenseWarningDays | Uns32 | Specify the number of days before a license expires to start issuing a warning. 0 disables warnings. |
| MIPS_UHI | Boolean | Enable MIPS-Unified Hosting interface |
| mipsUhiArgs | String | Specifies UHI arguments string separated by spaces |
| mipsUhiJail | String | Specifies UHI jailroot |
| MIPS_DV_MODE | Boolean | Enable Design Verification mode |
| MIPS_MAGIC_OPCODES | Boolean | Enable MIPS-specific magic Pass/Fail opcodes |
| enableTrickbox | Boolean | Enable trickbox addresses (specific for AVP) |
| fpucxdisable | Boolean | Disable FPU exceptions |

| | | |
|---------------------|-------------|--|
| TRU_PRESENT | Boolean | Disable or Enable based on TRU presence to control certain fields (e.x.perfCtl.PCTD) |
| ucLLwordsLocked | Uns32 | Numbers of words (4 byte) an uncached LL is locking. Maximum: 4K |
| FUSA | Boolean | Enable Functional Safety |
| CPC_FAULT_SUPPORTED | Uns32 | Specify the value for Functional Safety Supported register |
| CPC_FAULT_ENABLE | Uns32 | Specify the value for Functional Safety Enable register |
| cop2Bits | Uns32 | Specifies width in bits of COP2 registers (32 or 64) |
| cop2FileName | String | Specifies COP2 dynamically-loaded object (.so/.dll) defining COP2 instructions |
| udiConfig | Int32 | Specifies UDI configuration attribute |
| udiFileName | String | Specifies UDI dynamically-loaded object (.so/.dll) defining UDI instructions |
| vectoredinterrupt | Boolean | Enables vectored interrupts (sets Config3 VInt) |
| externalinterrupt | Boolean | Enables the use of an external interrupt controller (sets Config3 VEIC) |
| rootFixedMMU | Boolean | Override the root MMU type to fixed mapping when true (sets Config.MT=3 and Config.KU/K23=2) |
| rootMMUSizeM1 | Uns32 | Override the root MMUSizeM1 field in Config1 register (number of MMU entries-1) |
| srscctlHSS | Uns32 | Override the HSS field in SRSCtl register (number of shadow register sets) |
| firPS | Uns32 | Override the PS field in FIR register |
| firHas2008 | Uns32 | Override the Has2008 field in FIR register |
| usePreciseFpu | Uns32 | Use the precise Floating Point emulation |
| simulateLite | Enumeration | Run Simulation with optimization. There are several optimizations which could be combined (NONE, FS, MA or FSMA) |
| pridCompanyOptions | Uns32 | Override the Company Options field in PRId register |
| pridRevision | Uns32 | Override the Revision field in PRId register |
| globalClusterNum | Uns32 | Override the ClusterNum field in GlobalNumber register |
| intctlIPTI | Uns32 | Override the IPTI field in IntCtl register |
| intctlIPFDC | Uns32 | Override the IPFDC field in IntCtl register |
| intctlIPPCI | Uns32 | Override the IPPCI field in IntCtl register |
| numWatch | Uns32 | Specify number of WatchLo/WatchHi register pairs |
| xconfigSpecified | Boolean | True if the configuration comes from a valid xconfig file |
| segcfg0PA | Uns32 | Set CFG0.PA field of SegCtl0 register |
| segcfg1PA | Uns32 | Set CFG1.PA field of SegCtl0 register |
| segcfg2PA | Uns32 | Set CFG2.PA field of SegCtl1 register |
| segcfg3PA | Uns32 | Set CFG3.PA field of SegCtl1 register |
| segcfg4PA | Uns32 | Set CFG4.PA field of SegCtl2 register |
| segcfg5PA | Uns32 | Set CFG5.PA field of SegCtl2 register |
| segcfg0AM | Uns32 | Set CFG0.AM field of SegCtl0 register |
| segcfg1AM | Uns32 | Set CFG1.AM field of SegCtl0 register |
| segcfg2AM | Uns32 | Set CFG2.AM field of SegCtl1 register |
| segcfg3AM | Uns32 | Set CFG3.AM field of SegCtl1 register |
| segcfg4AM | Uns32 | Set CFG4.AM field of SegCtl2 register |
| segcfg5AM | Uns32 | Set CFG5.AM field of SegCtl2 register |
| segcfg0EU | Uns32 | Set CFG0.EU field of SegCtl0 register |
| segcfg1EU | Uns32 | Set CFG1.EU field of SegCtl0 register |
| segcfg2EU | Uns32 | Set CFG2.EU field of SegCtl1 register |
| segcfg3EU | Uns32 | Set CFG3.EU field of SegCtl1 register |
| segcfg4EU | Uns32 | Set CFG4.EU field of SegCtl2 register |
| segcfg5EU | Uns32 | Set CFG5.EU field of SegCtl2 register |
| segcfg0C | Uns32 | Set CFG0.C field of SegCtl0 register |
| segcfg1C | Uns32 | Set CFG1.C field of SegCtl0 register |

| | | |
|-----------------------|---------|---|
| segcfg2C | Uns32 | Set CFG2.C field of SegCtl1 register |
| segcfg3C | Uns32 | Set CFG3.C field of SegCtl1 register |
| segcfg4C | Uns32 | Set CFG4.C field of SegCtl2 register |
| segcfg5C | Uns32 | Set CFG5.C field of SegCtl2 register |
| cdmmSize | Uns32 | Override the cdmmSize reset value |
| configAR | Uns32 | Enables R6 support |
| configBM | Uns32 | Override the BM field in Config register (burst mode) |
| configDSP | Boolean | Override Config.DSP (data scratchpad RAM present) |
| configISP | Boolean | Override Config.ISP (instruction scratchpad RAM present) |
| configK0 | Uns32 | Override power on value of Config.K0 (set Kseg0 cacheability) |
| configKU | Uns32 | Override power on value of Config.KU (set Useg cacheability) |
| configK23 | Uns32 | Override power on value of Config.K23 (set Kseg23 cacheability) |
| configMDU | Boolean | Override Config.MDU (iterative multiply/divide unit) |
| configMM | Boolean | Override Config.MM (merging mode for write) |
| configMT | Uns32 | Override Config.MT |
| configSB | Boolean | Override Config.SB (simple bus transfers only) |
| configBCP | Boolean | Override Config.BCP (Buffer Cache Present) |
| MIPS16eASE | Boolean | Override Config1.CA (enables the MIPS16e ASE) |
| config1DA | Uns32 | Override Config1.DA (Dcache associativity) |
| config1DL | Uns32 | Override Config1.DL (Dcache line size) |
| config1DS | Uns32 | Override Config1.DS (Dcache sets per way) |
| config1EP | Boolean | Override Config1.EP (EJTag present) |
| config1IA | Uns32 | Override Config1.IA (Icache associativity) |
| config1IL | Uns32 | Override Config1.IL (Icache line size) |
| config1IS | Uns32 | Override Config1.IS (Icache sets per way) |
| config1MMUSizeM1 | Uns32 | Override Config1.MMUSizeM1 (number of MMU entries-1) |
| config1MMUSizeM1_VPE1 | Uns32 | Override Config1.MMUSizeM1 for VPE1 |
| config1MMUSizeM1_VPE2 | Uns32 | Override Config1.MMUSizeM1 for VPE2 |
| config1MMUSizeM1_VPE3 | Uns32 | Override Config1.MMUSizeM1 for VPE3 |
| config1WR | Boolean | Override Config1.WR (watchpoint registers present) |
| config1PC | Boolean | Override Config1.PC (Performance Counters present) |
| config1C2 | Boolean | Override Config1.C2 (Coprocessor 2 present) |
| config2SU | Uns32 | Override the SU field in Config2 register |
| config2SS | Uns32 | Override the SS field in Config2 register |
| config2SL | Uns32 | Override the SL field in Config2 register |
| config2SA | Uns32 | Override the SA field in Config2 register |
| config3BI | Boolean | Override Config3.BI |
| config3BP | Boolean | Override Config3.BP |
| config3CDMM | Boolean | Override Config3.CDMM |
| config3CTXTC | Boolean | Override Config3.CTXTC |
| config3DSPP | Boolean | Override Config3.DSPP |
| config3DSP2P | Boolean | Override Config3.DSP2P |
| config3IPLW | Uns32 | Override Config3.IPLW |
| config3ISA | Uns32 | Override Config3.ISA |
| config3ISAOnExc | Boolean | Override Config3.ISAOnExc |
| config3ITL | Boolean | Override Config3.ITL |
| config3LPA | Boolean | Override Config3.LPA |
| config3MCU | Boolean | Override Config3.MCU |
| config3MMAR | Uns32 | Override Config3.MMAR |
| config3RXI | Boolean | Override Config3.RXI |
| config3SC | Boolean | Override Config3.SC |

| | | |
|--------------------|---------|--|
| config3ULRI | Boolean | Override Config3.ULRI |
| config3VZ | Boolean | Override Config3.VZ |
| config3MSAP | Boolean | Override Config3.MSAP |
| config3CMGCR | Boolean | Override the CMGCR field in Config3 register |
| config3SP | Boolean | Override the SP field in Config3 register |
| config3TL | Uns32 | Override the TL field in Config3 register |
| config3PW | Boolean | Override the PW field in Config3 register |
| config4AE | Boolean | Override Config4.AE |
| config4IE | Uns32 | Override Config4.IE |
| config4MMUConfig | Uns32 | Override Config4.MMUConfig field (interpretation depends on MMUExtDef value) |
| config4MMUExtDef | Uns32 | Override Config4.MMUExtDef |
| config4VTLBSizeExt | Uns32 | Override Config4.VTLBSizeExt |
| config4KScrExist | Uns32 | Override Config4.KScrExist |
| config5EVA | Boolean | Override Config5.EVA |
| config5LLB | Boolean | Override Config5.LLB (LLAddr supports LLbit) |
| config5MRP | Boolean | Override Config5.MRP (MaaR Present) |
| config5NFExists | Boolean | Override Config5.NFExists |
| mips32Macro | Boolean | Enables the MIPS32 SAVE and RESTORE macro instructions. Ignored if Config5.CA2 is not set) |
| config5MSAEn | Boolean | Override Config5.MSAEn |
| config5MVH | Boolean | Override Config5.MVH (enable MTHC0 and MFHC0 instructions) |
| config5DEC | Boolean | Override Config5.DEC (to test Dual Endian Capability) |
| config5GI | Uns32 | Override Config5.GI (enable GINV) |
| config5CRCP | Boolean | Override Config5.CRCP (CRCP Present) |
| config5VP | Boolean | Override Config5.VP |
| config6FTLBEEn | Boolean | Override power on value of Config6.FTLBEEn |
| config7AR | Boolean | Override Config7.AR (Alias removed Data cache) |
| config7DCIDX_MODE | Uns32 | Override Config7.DCIDX_MODE |
| config7HCI | Boolean | Override Config7.HCI (Hardware Cache Initialization) |
| config7IAR | Boolean | Override Config7.IAR (Alias removed Instruction cache) |
| config7WII | Boolean | Override Config7.WII (wait IE/IXMT ignore) |
| config7ES | Uns32 | Override the ES field in Config7 register (Externalize sync) |
| config7WR | Boolean | Override Config7[31] bit (Alternative implementation of Watch registers) |
| config7FPR | Boolean | Override Config7.FPR (one-half FPU clock ratio) |
| config7USP | Uns32 | Override Config7.USP (USPRAM enable) |
| config7BTLM | Boolean | Override Config7.BTLM bit |
| config7BusSlp | Boolean | Override Config7.BusSlp bit |
| config7IVAD | Boolean | Override Config7.IVAD bit |
| config7RPS | Boolean | Override Config7.RPS bit |
| statusFR | Boolean | Override power on value in Status.FR (Floating point register mode) |
| fcsrABS2008 | Boolean | Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008) |
| fcsrNAN2008 | Boolean | Override FCSR.NAN2008 (QNaN/SNaN encodings match IEEE 754-2008 recommendation) |
| numMaarRegs | Uns32 | Override number of MAAR registers (must be even) |
| srsconf0SRS1 | Uns32 | Override the SRS1 field in SRSCnf0 register |
| srsconf0SRS2 | Uns32 | Override the SRS2 field in SRSCnf0 register |
| srsconf0SRS3 | Uns32 | Override the SRS3 field in SRSCnf0 register |
| wiredLimit | Uns32 | Override Limit field of the Wired register |
| wiredLimitBits | Uns32 | Override width of Limit field of the Wired register |
| wiredWiredBits | Uns32 | Override width of Wired field of the Wired register |
| cdmmBaseCI | Boolean | Override CDMMBase.CI |

| | | |
|------------------------------|-------------|--|
| parityEnable | Uns32 | Specify error detection support: 0 - none; 1 - parity; 2 - ECC |
| useMpTb | Boolean | Override Use of multi-processor test bench |
| ExceptionBase | Uns32 | Specify the BEV Exception Base address. (use GCR_Cx.RESET_BASE on CMP processors) |
| UseExceptionBase | Boolean | Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits |
| firstBEVExceptionBaseMaskBit | Uns32 | Specify LSB position of GCR_Cx.RESET_EXT_BASE.BEVExceptionBaseMask field. Only used when SegCtl present |
| EVAReset | Boolean | Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present |
| ExceptionBaseMask | Uns32 | Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present |
| ExceptionBasePA | Uns32 | Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present |
| l1BufferCache | Boolean | L1 Buffer Cache |
| EIC_OPTION | Uns32 | Override the external interrupt controller EIC_OPTION |
| guestCtl0RI | Uns32 | Override the RI field in GuestCtl0 register |
| guestCtl0MC | Uns32 | Override the MC field in GuestCtl0 register |
| guestCtl0CP0 | Uns32 | Override the CP0 field in GuestCtl0 register |
| guestCtl0AT | Uns32 | Override the AT field in GuestCtl0 register |
| guestCtl0GT | Uns32 | Override the GT field in GuestCtl0 register |
| guestCtl0CG | Uns32 | Override the CG field in GuestCtl0 register |
| guestCtl0CF | Uns32 | Override the CF field in GuestCtl0 register |
| guestCtl0G1 | Uns32 | Override the G1 field in GuestCtl0 register |
| guestCtl0RAD | Uns32 | Override the RAD field in GuestCtl0 register |
| guestCtl0DRG | Uns32 | Override the DRG field in GuestCtl0 register |
| hasImpl17 | Boolean | Enable read/write of Impl17 bit in Status register |
| hasImpl16 | Boolean | Enable read/write of Impl16 bit in Status register |
| guestintctlIPTI | Uns32 | Override the Guest IPTI field in IntCtl register |
| guestintctlIPFDC | Uns32 | Override the Guest IPFDC field in IntCtl register |
| guestintctlIPPCI | Uns32 | Override the Guest IPPCI field in IntCtl register |
| ISPRAM_SIZE | Uns32 | Encoded size of the ISPRAM region ($\log_2(\text{ISPRAM size in bytes}) - 11$) |
| ISPRAM_BASE | Uns64 | Starting physical address of the ISPRAM region |
| ISPRAM_ENABLE | Boolean | Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset) |
| ISPRAM_FILE | String | Load a MIPS hex file into the ISPRAM region prior to reset |
| DSPRAM_SIZE | Uns32 | Encoded size of the DSPRAM region ($\log_2(\text{DSPRAM size in bytes}) - 11$) |
| DSPRAM_BASE | Uns64 | Starting physical address of the DSPRAM region |
| DSPRAM_ENABLE | Boolean | Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset) |
| DSPRAM_PRESENT | Boolean | DSPRAM is present with SAAR |
| USPRAM_SIZE | Uns32 | Encoded size of the USPRAM region ($\log_2(\text{USPRAM size in bytes}) - 11$) |
| USPRAM_BASE | Uns64 | Starting physical address of the USPRAM region |
| USPRAM_ENABLE | Boolean | Set the enable bit of the USPRAM region's tag (used to enable the USPRAM region prior to reset) |
| USPRAM_FILE | String | Load a MIPS hex file into the USPRAM region prior to reset |
| misalignedDataException | Enumeration | Select misaligned data access exception signaling: never, checkCCA or always (never, checkCCA or always) |

| | | |
|---------------|---------|---|
| commitTlbwErr | Boolean | Commit TLBWI/TLBRI on ECC; in MIPS_DV_MODE only |
|---------------|---------|---|

Table 8.1: Parameters that can be set in: CPU

Chapter 9

Execution Modes

| Mode | Code |
|------------------|------|
| KERNEL | 0 |
| DEBUG | 1 |
| SUPERVISOR | 2 |
| USER | 3 |
| GUEST_KERNEL | 4 |
| GUEST_SUPERVISOR | 5 |
| GUEST_USER | 6 |

Table 9.1: Modes implemented in: CPU

Chapter 10

Exceptions

| Exception | Code |
|-----------|------|
| Int | 0 |
| Mod | 1 |
| TLBL | 2 |
| TLBS | 3 |
| AdEL | 4 |
| AdES | 5 |
| IBE | 6 |
| DBE | 7 |
| Sys | 8 |
| Bp | 9 |
| RI | 10 |
| CpU | 11 |
| Ov | 12 |
| Tr | 13 |
| FPE | 15 |
| Impl1 | 16 |
| Impl2 | 17 |
| C2E | 18 |
| TLBRI | 19 |
| TLBXI | 20 |
| MDMX | 22 |
| WATCH | 23 |
| MCheck | 24 |
| Thread | 25 |
| DSPDis | 26 |
| GE | 27 |
| Prot | 29 |
| CacheErr | 30 |

Table 10.1: Exceptions implemented in: CPU

Chapter 11

Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

11.1 Level 1: CPU

This level in the model hierarchy has 20 commands.

This level in the model hierarchy has 7 register groups:

| Group name | Registers |
|---------------------|-----------|
| Core | 65 |
| FPU | 34 |
| DSP | 9 |
| Shadow | 1024 |
| COP0 | 126 |
| SPRAM | 15 |
| Integration_support | 1 |

Table 11.1: Register groups

This level in the model hierarchy has no children.

Chapter 12

Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

12.1 Level 1: CPU

12.1.1 isync

specify instruction address range for synchronous execution

| Argument | Type | Description |
|------------|-------|--|
| -addresshi | Uns64 | end address of synchronous execution range |
| -addresslo | Uns64 | start address of synchronous execution range |

Table 12.1: isync command arguments

12.1.2 itrace

enable or disable instruction tracing

| Argument | Type | Description |
|-------------------|---------|--|
| -after | Uns64 | apply after this many instructions |
| -enable | Boolean | enable instruction tracing |
| -instructioncount | Boolean | include the instruction number in each trace |
| -off | Boolean | disable instruction tracing |
| -on | Boolean | enable instruction tracing |
| -registerchange | Boolean | show registers changed by this instruction |
| -registers | Boolean | show registers after each trace |

Table 12.2: itrace command arguments

12.1.3 mipsCOP0

query a COP0 register value using <register><select>

| Argument | Type | Description |
|-----------|-------|------------------------------------|
| -register | Uns32 | specify the COP0 register resource |

| | | |
|---------|-------|----------------------------------|
| -select | Uns32 | specify the COP0 register select |
|---------|-------|----------------------------------|

Table 12.3: mipsCOP0 command arguments

12.1.4 mipsCacheDisable

12.1.4.1 Argument description

Disables tag or full cache model

12.1.5 mipsCacheEnable

enable tag or full cache model

| Argument | Type | Description |
|----------|---------|----------------------------------|
| -debug | Int32 | set cache model debug flags |
| -full | Boolean | enable full cache model |
| -tag | Boolean | enable cache tag line only model |

Table 12.4: mipsCacheEnable command arguments

12.1.6 mipsCacheRatio

Report current hit ratio for selected cache

| Argument | Type | Description |
|----------|---------|-----------------------------|
| -dcache | Boolean | report hit ratio for dcache |
| -icache | Boolean | report hit ratio for icache |

Table 12.5: mipsCacheRatio command arguments

12.1.7 mipsCacheReport

12.1.7.1 Argument description

Report current cache statistics

12.1.8 mipsCacheReset

12.1.8.1 Argument description

reset the cache model

12.1.9 mipsCacheTrace

Control the tracing of cache accesses

| Argument | Type | Description |
|-------------|---------|-------------|
| -noartifact | Boolean | |
| -nocached | Boolean | |
| -nodcache | Boolean | |

| | | |
|-------------|---------|----------------------------|
| -noicache | Boolean | |
| -notrue | Boolean | |
| -nouncached | Boolean | |
| -off | Boolean | turn off the cache tracing |
| -on | Boolean | turn on the cache tracing |

Table 12.6: mipsCacheTrace command arguments

12.1.10 mipsDebugFlags

Set the mips model debug value

| Argument | Type | Description |
|----------|-------|--------------------------------|
| -value | Uns32 | specify mips model debug flags |

Table 12.7: mipsDebugFlags command arguments

12.1.11 mipsReadRegister

Read processor register using <resource><offset>

| Argument | Type | Description |
|-----------|-------|-----------------------|
| -offset | Uns32 | the register offset |
| -resource | Uns32 | the register resource |

Table 12.8: mipsReadRegister command arguments

12.1.12 mipsReadTLBEntry

read a TLB entry specified by the index

| Argument | Type | Description |
|----------|-------|----------------------|
| -index | Uns64 | select the TLB entry |

Table 12.9: mipsReadTLBEntry command arguments

12.1.13 mipsTLBDump

12.1.13.1 Argument description

Dumps the current contents of the TLB

12.1.14 mipsTLBDumpGuest

12.1.14.1 Argument description

Dumps the current contents of the Guest TLB

12.1.15 mipsTLBDumpRoot

12.1.15.1 Argument description

Dumps the current contents of the Root TLB

12.1.16 mipsTLBGetPhys

Reports the entry(s) in the TLB that match the given virtual address and ASID

| Argument | Type | Description |
|----------|-------|-----------------|
| -asid | Uns64 | ASID |
| -va | Uns64 | virtual address |

Table 12.10: mipsTLBGetPhys command arguments

12.1.17 mipsTraceGuest

control tracing of guest

| Argument | Type | Description |
|----------|---------|---------------|
| -off | Boolean | stop tracing |
| -on | Boolean | start tracing |

Table 12.11: mipsTraceGuest command arguments

12.1.18 mipsTraceRoot

control tracing on root processor

| Argument | Type | Description |
|----------|---------|---------------|
| -off | Boolean | stop tracing |
| -on | Boolean | start tracing |

Table 12.12: mipsTraceRoot command arguments

12.1.19 mipsWriteRegister

Write processor register using <resource><offset><value>

| Argument | Type | Description |
|-----------|-------|--------------------------------|
| -offset | Uns32 | the register offset |
| -resource | Uns32 | the register resource |
| -value | Uns64 | the value to write to register |

Table 12.13: mipsWriteRegister command arguments

12.1.20 mipsWriteTLBEntry

Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

| Argument | Type | Description |
|-----------------|-------|-----------------------------|
| -hi0 | Uns64 | the TLB entry high address |
| -index | Uns64 | the TLB entry index |
| -lo0 | Uns64 | the TLB entry low address 0 |
| -lo1 | Uns64 | the TLB entry low address 1 |
| -mask | Uns64 | the TLB entry mask |

Table 12.14: mipsWriteTLBEntry command arguments

Chapter 13

Registers

13.1 Level 1: CPU

13.1.1 Core

Registers at level:1, type:CPU group:Core

| Name | Bits | Initial-Hex | RW | Description |
|------|------|-------------|----|-----------------|
| zero | 32 | 0 | r- | constant zero |
| at | 32 | 0 | rw | |
| v0 | 32 | 0 | rw | |
| v1 | 32 | 0 | rw | |
| a0 | 32 | 0 | rw | |
| a1 | 32 | 0 | rw | |
| a2 | 32 | 0 | rw | |
| a3 | 32 | 0 | rw | |
| t0 | 32 | 0 | rw | |
| t1 | 32 | 0 | rw | |
| t2 | 32 | 0 | rw | |
| t3 | 32 | 0 | rw | |
| t4 | 32 | 0 | rw | |
| t5 | 32 | 0 | rw | |
| t6 | 32 | 0 | rw | |
| t7 | 32 | 0 | rw | |
| s0 | 32 | 0 | rw | |
| s1 | 32 | 0 | rw | |
| s2 | 32 | 0 | rw | |
| s3 | 32 | 0 | rw | |
| s4 | 32 | 0 | rw | |
| s5 | 32 | 0 | rw | |
| s6 | 32 | 0 | rw | |
| s7 | 32 | 0 | rw | |
| t8 | 32 | 0 | rw | |
| t9 | 32 | 0 | rw | |
| k0 | 32 | 0 | rw | |
| k1 | 32 | 0 | rw | |
| gp | 32 | 0 | rw | |
| sp | 32 | 0 | rw | stack pointer |
| s8 | 32 | 0 | rw | frame pointer |
| ra | 32 | 0 | rw | |
| pc | 32 | bfc00000 | rw | program counter |
| r0 | 32 | 0 | r- | constant zero |

| | | | | |
|-----|----|---|----|---------------|
| r1 | 32 | 0 | rw | |
| r2 | 32 | 0 | rw | |
| r3 | 32 | 0 | rw | |
| r4 | 32 | 0 | rw | |
| r5 | 32 | 0 | rw | |
| r6 | 32 | 0 | rw | |
| r7 | 32 | 0 | rw | |
| r8 | 32 | 0 | rw | |
| r9 | 32 | 0 | rw | |
| r10 | 32 | 0 | rw | |
| r11 | 32 | 0 | rw | |
| r12 | 32 | 0 | rw | |
| r13 | 32 | 0 | rw | |
| r14 | 32 | 0 | rw | |
| r15 | 32 | 0 | rw | |
| r16 | 32 | 0 | rw | |
| r17 | 32 | 0 | rw | |
| r18 | 32 | 0 | rw | |
| r19 | 32 | 0 | rw | |
| r20 | 32 | 0 | rw | |
| r21 | 32 | 0 | rw | |
| r22 | 32 | 0 | rw | |
| r23 | 32 | 0 | rw | |
| r24 | 32 | 0 | rw | |
| r25 | 32 | 0 | rw | |
| r26 | 32 | 0 | rw | |
| r27 | 32 | 0 | rw | |
| r28 | 32 | 0 | rw | |
| r29 | 32 | 0 | rw | stack pointer |
| r30 | 32 | 0 | rw | frame pointer |
| r31 | 32 | 0 | rw | |

Table 13.1: Registers at level 1, type:CPU group:Core

13.1.2 FPU

Registers at level:1, type:CPU group:FPU

| Name | Bits | Initial-Hex | RW | Description |
|------|------|-------------|----|-------------|
| f0 | 32 | 0 | rw | |
| f1 | 32 | 0 | rw | |
| f2 | 32 | 0 | rw | |
| f3 | 32 | 0 | rw | |
| f4 | 32 | 0 | rw | |
| f5 | 32 | 0 | rw | |
| f6 | 32 | 0 | rw | |
| f7 | 32 | 0 | rw | |
| f8 | 32 | 0 | rw | |
| f9 | 32 | 0 | rw | |
| f10 | 32 | 0 | rw | |
| f11 | 32 | 0 | rw | |
| f12 | 32 | 0 | rw | |
| f13 | 32 | 0 | rw | |
| f14 | 32 | 0 | rw | |
| f15 | 32 | 0 | rw | |
| f16 | 32 | 0 | rw | |

| | | | | |
|-----|----|----------|----|----------------------------|
| f17 | 32 | 0 | rw | |
| f18 | 32 | 0 | rw | |
| f19 | 32 | 0 | rw | |
| f20 | 32 | 0 | rw | |
| f21 | 32 | 0 | rw | |
| f22 | 32 | 0 | rw | |
| f23 | 32 | 0 | rw | |
| f24 | 32 | 0 | rw | |
| f25 | 32 | 0 | rw | |
| f26 | 32 | 0 | rw | |
| f27 | 32 | 0 | rw | |
| f28 | 32 | 0 | rw | |
| f29 | 32 | 0 | rw | |
| f30 | 32 | 0 | rw | |
| f31 | 32 | 0 | rw | |
| fsr | 32 | 10c0000 | rw | floating point status |
| fir | 32 | 11f3a720 | r- | floating point information |

Table 13.2: Registers at level 1, type:CPU group:FPU

13.1.3 DSP

Registers at level:1, type:CPU group:DSP

| Name | Bits | Initial-Hex | RW | Description |
|--------|------|-------------|----|-------------|
| lo | 32 | 0 | rw | |
| hi | 32 | 0 | rw | |
| lo1 | 32 | 0 | rw | |
| hi1 | 32 | 0 | rw | |
| lo2 | 32 | 0 | rw | |
| hi2 | 32 | 0 | rw | |
| lo3 | 32 | 0 | rw | |
| hi3 | 32 | 0 | rw | |
| dspctl | 32 | 0 | rw | DSP control |

Table 13.3: Registers at level 1, type:CPU group:DSP

13.1.4 Shadow

Registers at level:1, type:CPU group:Shadow

| Name | Bits | Initial-Hex | RW | Description |
|---------|------|-------------|----|---------------|
| zero[0] | 32 | 0 | r- | constant zero |
| at[0] | 32 | 0 | rw | |
| v0[0] | 32 | 0 | rw | |
| v1[0] | 32 | 0 | rw | |
| a0[0] | 32 | 0 | rw | |
| a1[0] | 32 | 0 | rw | |
| a2[0] | 32 | 0 | rw | |
| a3[0] | 32 | 0 | rw | |
| t0[0] | 32 | 0 | rw | |
| t1[0] | 32 | 0 | rw | |
| t2[0] | 32 | 0 | rw | |
| t3[0] | 32 | 0 | rw | |
| t4[0] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| t5[0] | 32 | 0 | rw | |
| t6[0] | 32 | 0 | rw | |
| t7[0] | 32 | 0 | rw | |
| s0[0] | 32 | 0 | rw | |
| s1[0] | 32 | 0 | rw | |
| s2[0] | 32 | 0 | rw | |
| s3[0] | 32 | 0 | rw | |
| s4[0] | 32 | 0 | rw | |
| s5[0] | 32 | 0 | rw | |
| s6[0] | 32 | 0 | rw | |
| s7[0] | 32 | 0 | rw | |
| t8[0] | 32 | 0 | rw | |
| t9[0] | 32 | 0 | rw | |
| k0[0] | 32 | 0 | rw | |
| k1[0] | 32 | 0 | rw | |
| gp[0] | 32 | 0 | rw | |
| sp[0] | 32 | 0 | rw | stack pointer |
| s8[0] | 32 | 0 | rw | frame pointer |
| ra[0] | 32 | 0 | rw | |
| zero[1] | 32 | 0 | r- | constant zero |
| at[1] | 32 | 0 | rw | |
| v0[1] | 32 | 0 | rw | |
| v1[1] | 32 | 0 | rw | |
| a0[1] | 32 | 0 | rw | |
| a1[1] | 32 | 0 | rw | |
| a2[1] | 32 | 0 | rw | |
| a3[1] | 32 | 0 | rw | |
| t0[1] | 32 | 0 | rw | |
| t1[1] | 32 | 0 | rw | |
| t2[1] | 32 | 0 | rw | |
| t3[1] | 32 | 0 | rw | |
| t4[1] | 32 | 0 | rw | |
| t5[1] | 32 | 0 | rw | |
| t6[1] | 32 | 0 | rw | |
| t7[1] | 32 | 0 | rw | |
| s0[1] | 32 | 0 | rw | |
| s1[1] | 32 | 0 | rw | |
| s2[1] | 32 | 0 | rw | |
| s3[1] | 32 | 0 | rw | |
| s4[1] | 32 | 0 | rw | |
| s5[1] | 32 | 0 | rw | |
| s6[1] | 32 | 0 | rw | |
| s7[1] | 32 | 0 | rw | |
| t8[1] | 32 | 0 | rw | |
| t9[1] | 32 | 0 | rw | |
| k0[1] | 32 | 0 | rw | |
| k1[1] | 32 | 0 | rw | |
| gp[1] | 32 | 0 | rw | |
| sp[1] | 32 | 0 | rw | stack pointer |
| s8[1] | 32 | 0 | rw | frame pointer |
| ra[1] | 32 | 0 | rw | |
| zero[2] | 32 | 0 | r- | constant zero |
| at[2] | 32 | 0 | rw | |
| v0[2] | 32 | 0 | rw | |
| v1[2] | 32 | 0 | rw | |
| a0[2] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| a1[2] | 32 | 0 | rw | |
| a2[2] | 32 | 0 | rw | |
| a3[2] | 32 | 0 | rw | |
| t0[2] | 32 | 0 | rw | |
| t1[2] | 32 | 0 | rw | |
| t2[2] | 32 | 0 | rw | |
| t3[2] | 32 | 0 | rw | |
| t4[2] | 32 | 0 | rw | |
| t5[2] | 32 | 0 | rw | |
| t6[2] | 32 | 0 | rw | |
| t7[2] | 32 | 0 | rw | |
| s0[2] | 32 | 0 | rw | |
| s1[2] | 32 | 0 | rw | |
| s2[2] | 32 | 0 | rw | |
| s3[2] | 32 | 0 | rw | |
| s4[2] | 32 | 0 | rw | |
| s5[2] | 32 | 0 | rw | |
| s6[2] | 32 | 0 | rw | |
| s7[2] | 32 | 0 | rw | |
| t8[2] | 32 | 0 | rw | |
| t9[2] | 32 | 0 | rw | |
| k0[2] | 32 | 0 | rw | |
| k1[2] | 32 | 0 | rw | |
| gp[2] | 32 | 0 | rw | |
| sp[2] | 32 | 0 | rw | stack pointer |
| s8[2] | 32 | 0 | rw | frame pointer |
| ra[2] | 32 | 0 | rw | |
| zero[3] | 32 | 0 | r- | constant zero |
| at[3] | 32 | 0 | rw | |
| v0[3] | 32 | 0 | rw | |
| v1[3] | 32 | 0 | rw | |
| a0[3] | 32 | 0 | rw | |
| a1[3] | 32 | 0 | rw | |
| a2[3] | 32 | 0 | rw | |
| a3[3] | 32 | 0 | rw | |
| t0[3] | 32 | 0 | rw | |
| t1[3] | 32 | 0 | rw | |
| t2[3] | 32 | 0 | rw | |
| t3[3] | 32 | 0 | rw | |
| t4[3] | 32 | 0 | rw | |
| t5[3] | 32 | 0 | rw | |
| t6[3] | 32 | 0 | rw | |
| t7[3] | 32 | 0 | rw | |
| s0[3] | 32 | 0 | rw | |
| s1[3] | 32 | 0 | rw | |
| s2[3] | 32 | 0 | rw | |
| s3[3] | 32 | 0 | rw | |
| s4[3] | 32 | 0 | rw | |
| s5[3] | 32 | 0 | rw | |
| s6[3] | 32 | 0 | rw | |
| s7[3] | 32 | 0 | rw | |
| t8[3] | 32 | 0 | rw | |
| t9[3] | 32 | 0 | rw | |
| k0[3] | 32 | 0 | rw | |
| k1[3] | 32 | 0 | rw | |
| gp[3] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| sp[3] | 32 | 0 | rw | stack pointer |
| s8[3] | 32 | 0 | rw | frame pointer |
| ra[3] | 32 | 0 | rw | |
| zero[4] | 32 | 0 | r- | constant zero |
| at[4] | 32 | 0 | rw | |
| v0[4] | 32 | 0 | rw | |
| v1[4] | 32 | 0 | rw | |
| a0[4] | 32 | 0 | rw | |
| a1[4] | 32 | 0 | rw | |
| a2[4] | 32 | 0 | rw | |
| a3[4] | 32 | 0 | rw | |
| t0[4] | 32 | 0 | rw | |
| t1[4] | 32 | 0 | rw | |
| t2[4] | 32 | 0 | rw | |
| t3[4] | 32 | 0 | rw | |
| t4[4] | 32 | 0 | rw | |
| t5[4] | 32 | 0 | rw | |
| t6[4] | 32 | 0 | rw | |
| t7[4] | 32 | 0 | rw | |
| s0[4] | 32 | 0 | rw | |
| s1[4] | 32 | 0 | rw | |
| s2[4] | 32 | 0 | rw | |
| s3[4] | 32 | 0 | rw | |
| s4[4] | 32 | 0 | rw | |
| s5[4] | 32 | 0 | rw | |
| s6[4] | 32 | 0 | rw | |
| s7[4] | 32 | 0 | rw | |
| t8[4] | 32 | 0 | rw | |
| t9[4] | 32 | 0 | rw | |
| k0[4] | 32 | 0 | rw | |
| k1[4] | 32 | 0 | rw | |
| gp[4] | 32 | 0 | rw | |
| sp[4] | 32 | 0 | rw | stack pointer |
| s8[4] | 32 | 0 | rw | frame pointer |
| ra[4] | 32 | 0 | rw | |
| zero[5] | 32 | 0 | r- | constant zero |
| at[5] | 32 | 0 | rw | |
| v0[5] | 32 | 0 | rw | |
| v1[5] | 32 | 0 | rw | |
| a0[5] | 32 | 0 | rw | |
| a1[5] | 32 | 0 | rw | |
| a2[5] | 32 | 0 | rw | |
| a3[5] | 32 | 0 | rw | |
| t0[5] | 32 | 0 | rw | |
| t1[5] | 32 | 0 | rw | |
| t2[5] | 32 | 0 | rw | |
| t3[5] | 32 | 0 | rw | |
| t4[5] | 32 | 0 | rw | |
| t5[5] | 32 | 0 | rw | |
| t6[5] | 32 | 0 | rw | |
| t7[5] | 32 | 0 | rw | |
| s0[5] | 32 | 0 | rw | |
| s1[5] | 32 | 0 | rw | |
| s2[5] | 32 | 0 | rw | |
| s3[5] | 32 | 0 | rw | |
| s4[5] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| s5[5] | 32 | 0 | rw | |
| s6[5] | 32 | 0 | rw | |
| s7[5] | 32 | 0 | rw | |
| t8[5] | 32 | 0 | rw | |
| t9[5] | 32 | 0 | rw | |
| k0[5] | 32 | 0 | rw | |
| k1[5] | 32 | 0 | rw | |
| gp[5] | 32 | 0 | rw | |
| sp[5] | 32 | 0 | rw | stack pointer |
| s8[5] | 32 | 0 | rw | frame pointer |
| ra[5] | 32 | 0 | rw | |
| zero[6] | 32 | 0 | r- | constant zero |
| at[6] | 32 | 0 | rw | |
| v0[6] | 32 | 0 | rw | |
| v1[6] | 32 | 0 | rw | |
| a0[6] | 32 | 0 | rw | |
| a1[6] | 32 | 0 | rw | |
| a2[6] | 32 | 0 | rw | |
| a3[6] | 32 | 0 | rw | |
| t0[6] | 32 | 0 | rw | |
| t1[6] | 32 | 0 | rw | |
| t2[6] | 32 | 0 | rw | |
| t3[6] | 32 | 0 | rw | |
| t4[6] | 32 | 0 | rw | |
| t5[6] | 32 | 0 | rw | |
| t6[6] | 32 | 0 | rw | |
| t7[6] | 32 | 0 | rw | |
| s0[6] | 32 | 0 | rw | |
| s1[6] | 32 | 0 | rw | |
| s2[6] | 32 | 0 | rw | |
| s3[6] | 32 | 0 | rw | |
| s4[6] | 32 | 0 | rw | |
| s5[6] | 32 | 0 | rw | |
| s6[6] | 32 | 0 | rw | |
| s7[6] | 32 | 0 | rw | |
| t8[6] | 32 | 0 | rw | |
| t9[6] | 32 | 0 | rw | |
| k0[6] | 32 | 0 | rw | |
| k1[6] | 32 | 0 | rw | |
| gp[6] | 32 | 0 | rw | |
| sp[6] | 32 | 0 | rw | stack pointer |
| s8[6] | 32 | 0 | rw | frame pointer |
| ra[6] | 32 | 0 | rw | |
| zero[7] | 32 | 0 | r- | constant zero |
| at[7] | 32 | 0 | rw | |
| v0[7] | 32 | 0 | rw | |
| v1[7] | 32 | 0 | rw | |
| a0[7] | 32 | 0 | rw | |
| a1[7] | 32 | 0 | rw | |
| a2[7] | 32 | 0 | rw | |
| a3[7] | 32 | 0 | rw | |
| t0[7] | 32 | 0 | rw | |
| t1[7] | 32 | 0 | rw | |
| t2[7] | 32 | 0 | rw | |
| t3[7] | 32 | 0 | rw | |
| t4[7] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| t5[7] | 32 | 0 | rw | |
| t6[7] | 32 | 0 | rw | |
| t7[7] | 32 | 0 | rw | |
| s0[7] | 32 | 0 | rw | |
| s1[7] | 32 | 0 | rw | |
| s2[7] | 32 | 0 | rw | |
| s3[7] | 32 | 0 | rw | |
| s4[7] | 32 | 0 | rw | |
| s5[7] | 32 | 0 | rw | |
| s6[7] | 32 | 0 | rw | |
| s7[7] | 32 | 0 | rw | |
| t8[7] | 32 | 0 | rw | |
| t9[7] | 32 | 0 | rw | |
| k0[7] | 32 | 0 | rw | |
| k1[7] | 32 | 0 | rw | |
| gp[7] | 32 | 0 | rw | |
| sp[7] | 32 | 0 | rw | stack pointer |
| s8[7] | 32 | 0 | rw | frame pointer |
| ra[7] | 32 | 0 | rw | |
| zero[8] | 32 | 0 | r- | constant zero |
| at[8] | 32 | 0 | rw | |
| v0[8] | 32 | 0 | rw | |
| v1[8] | 32 | 0 | rw | |
| a0[8] | 32 | 0 | rw | |
| a1[8] | 32 | 0 | rw | |
| a2[8] | 32 | 0 | rw | |
| a3[8] | 32 | 0 | rw | |
| t0[8] | 32 | 0 | rw | |
| t1[8] | 32 | 0 | rw | |
| t2[8] | 32 | 0 | rw | |
| t3[8] | 32 | 0 | rw | |
| t4[8] | 32 | 0 | rw | |
| t5[8] | 32 | 0 | rw | |
| t6[8] | 32 | 0 | rw | |
| t7[8] | 32 | 0 | rw | |
| s0[8] | 32 | 0 | rw | |
| s1[8] | 32 | 0 | rw | |
| s2[8] | 32 | 0 | rw | |
| s3[8] | 32 | 0 | rw | |
| s4[8] | 32 | 0 | rw | |
| s5[8] | 32 | 0 | rw | |
| s6[8] | 32 | 0 | rw | |
| s7[8] | 32 | 0 | rw | |
| t8[8] | 32 | 0 | rw | |
| t9[8] | 32 | 0 | rw | |
| k0[8] | 32 | 0 | rw | |
| k1[8] | 32 | 0 | rw | |
| gp[8] | 32 | 0 | rw | |
| sp[8] | 32 | 0 | rw | stack pointer |
| s8[8] | 32 | 0 | rw | frame pointer |
| ra[8] | 32 | 0 | rw | |
| zero[9] | 32 | 0 | r- | constant zero |
| at[9] | 32 | 0 | rw | |
| v0[9] | 32 | 0 | rw | |
| v1[9] | 32 | 0 | rw | |
| a0[9] | 32 | 0 | rw | |

| | | | | |
|----------|----|---|----|---------------|
| a1[9] | 32 | 0 | rw | |
| a2[9] | 32 | 0 | rw | |
| a3[9] | 32 | 0 | rw | |
| t0[9] | 32 | 0 | rw | |
| t1[9] | 32 | 0 | rw | |
| t2[9] | 32 | 0 | rw | |
| t3[9] | 32 | 0 | rw | |
| t4[9] | 32 | 0 | rw | |
| t5[9] | 32 | 0 | rw | |
| t6[9] | 32 | 0 | rw | |
| t7[9] | 32 | 0 | rw | |
| s0[9] | 32 | 0 | rw | |
| s1[9] | 32 | 0 | rw | |
| s2[9] | 32 | 0 | rw | |
| s3[9] | 32 | 0 | rw | |
| s4[9] | 32 | 0 | rw | |
| s5[9] | 32 | 0 | rw | |
| s6[9] | 32 | 0 | rw | |
| s7[9] | 32 | 0 | rw | |
| t8[9] | 32 | 0 | rw | |
| t9[9] | 32 | 0 | rw | |
| k0[9] | 32 | 0 | rw | |
| k1[9] | 32 | 0 | rw | |
| gp[9] | 32 | 0 | rw | |
| sp[9] | 32 | 0 | rw | stack pointer |
| s8[9] | 32 | 0 | rw | frame pointer |
| ra[9] | 32 | 0 | rw | |
| zero[10] | 32 | 0 | r- | constant zero |
| at[10] | 32 | 0 | rw | |
| v0[10] | 32 | 0 | rw | |
| v1[10] | 32 | 0 | rw | |
| a0[10] | 32 | 0 | rw | |
| a1[10] | 32 | 0 | rw | |
| a2[10] | 32 | 0 | rw | |
| a3[10] | 32 | 0 | rw | |
| t0[10] | 32 | 0 | rw | |
| t1[10] | 32 | 0 | rw | |
| t2[10] | 32 | 0 | rw | |
| t3[10] | 32 | 0 | rw | |
| t4[10] | 32 | 0 | rw | |
| t5[10] | 32 | 0 | rw | |
| t6[10] | 32 | 0 | rw | |
| t7[10] | 32 | 0 | rw | |
| s0[10] | 32 | 0 | rw | |
| s1[10] | 32 | 0 | rw | |
| s2[10] | 32 | 0 | rw | |
| s3[10] | 32 | 0 | rw | |
| s4[10] | 32 | 0 | rw | |
| s5[10] | 32 | 0 | rw | |
| s6[10] | 32 | 0 | rw | |
| s7[10] | 32 | 0 | rw | |
| t8[10] | 32 | 0 | rw | |
| t9[10] | 32 | 0 | rw | |
| k0[10] | 32 | 0 | rw | |
| k1[10] | 32 | 0 | rw | |
| gp[10] | 32 | 0 | rw | |

| | | | | |
|----------|----|---|----|---------------|
| sp[10] | 32 | 0 | rw | stack pointer |
| s8[10] | 32 | 0 | rw | frame pointer |
| ra[10] | 32 | 0 | rw | |
| zero[11] | 32 | 0 | r- | constant zero |
| at[11] | 32 | 0 | rw | |
| v0[11] | 32 | 0 | rw | |
| v1[11] | 32 | 0 | rw | |
| a0[11] | 32 | 0 | rw | |
| a1[11] | 32 | 0 | rw | |
| a2[11] | 32 | 0 | rw | |
| a3[11] | 32 | 0 | rw | |
| t0[11] | 32 | 0 | rw | |
| t1[11] | 32 | 0 | rw | |
| t2[11] | 32 | 0 | rw | |
| t3[11] | 32 | 0 | rw | |
| t4[11] | 32 | 0 | rw | |
| t5[11] | 32 | 0 | rw | |
| t6[11] | 32 | 0 | rw | |
| t7[11] | 32 | 0 | rw | |
| s0[11] | 32 | 0 | rw | |
| s1[11] | 32 | 0 | rw | |
| s2[11] | 32 | 0 | rw | |
| s3[11] | 32 | 0 | rw | |
| s4[11] | 32 | 0 | rw | |
| s5[11] | 32 | 0 | rw | |
| s6[11] | 32 | 0 | rw | |
| s7[11] | 32 | 0 | rw | |
| t8[11] | 32 | 0 | rw | |
| t9[11] | 32 | 0 | rw | |
| k0[11] | 32 | 0 | rw | |
| k1[11] | 32 | 0 | rw | |
| gp[11] | 32 | 0 | rw | |
| sp[11] | 32 | 0 | rw | stack pointer |
| s8[11] | 32 | 0 | rw | frame pointer |
| ra[11] | 32 | 0 | rw | |
| zero[12] | 32 | 0 | r- | constant zero |
| at[12] | 32 | 0 | rw | |
| v0[12] | 32 | 0 | rw | |
| v1[12] | 32 | 0 | rw | |
| a0[12] | 32 | 0 | rw | |
| a1[12] | 32 | 0 | rw | |
| a2[12] | 32 | 0 | rw | |
| a3[12] | 32 | 0 | rw | |
| t0[12] | 32 | 0 | rw | |
| t1[12] | 32 | 0 | rw | |
| t2[12] | 32 | 0 | rw | |
| t3[12] | 32 | 0 | rw | |
| t4[12] | 32 | 0 | rw | |
| t5[12] | 32 | 0 | rw | |
| t6[12] | 32 | 0 | rw | |
| t7[12] | 32 | 0 | rw | |
| s0[12] | 32 | 0 | rw | |
| s1[12] | 32 | 0 | rw | |
| s2[12] | 32 | 0 | rw | |
| s3[12] | 32 | 0 | rw | |
| s4[12] | 32 | 0 | rw | |

| | | | | |
|----------|----|---|----|---------------|
| s5[12] | 32 | 0 | rw | |
| s6[12] | 32 | 0 | rw | |
| s7[12] | 32 | 0 | rw | |
| t8[12] | 32 | 0 | rw | |
| t9[12] | 32 | 0 | rw | |
| k0[12] | 32 | 0 | rw | |
| k1[12] | 32 | 0 | rw | |
| gp[12] | 32 | 0 | rw | |
| sp[12] | 32 | 0 | rw | stack pointer |
| s8[12] | 32 | 0 | rw | frame pointer |
| ra[12] | 32 | 0 | rw | |
| zero[13] | 32 | 0 | r- | constant zero |
| at[13] | 32 | 0 | rw | |
| v0[13] | 32 | 0 | rw | |
| v1[13] | 32 | 0 | rw | |
| a0[13] | 32 | 0 | rw | |
| a1[13] | 32 | 0 | rw | |
| a2[13] | 32 | 0 | rw | |
| a3[13] | 32 | 0 | rw | |
| t0[13] | 32 | 0 | rw | |
| t1[13] | 32 | 0 | rw | |
| t2[13] | 32 | 0 | rw | |
| t3[13] | 32 | 0 | rw | |
| t4[13] | 32 | 0 | rw | |
| t5[13] | 32 | 0 | rw | |
| t6[13] | 32 | 0 | rw | |
| t7[13] | 32 | 0 | rw | |
| s0[13] | 32 | 0 | rw | |
| s1[13] | 32 | 0 | rw | |
| s2[13] | 32 | 0 | rw | |
| s3[13] | 32 | 0 | rw | |
| s4[13] | 32 | 0 | rw | |
| s5[13] | 32 | 0 | rw | |
| s6[13] | 32 | 0 | rw | |
| s7[13] | 32 | 0 | rw | |
| t8[13] | 32 | 0 | rw | |
| t9[13] | 32 | 0 | rw | |
| k0[13] | 32 | 0 | rw | |
| k1[13] | 32 | 0 | rw | |
| gp[13] | 32 | 0 | rw | |
| sp[13] | 32 | 0 | rw | stack pointer |
| s8[13] | 32 | 0 | rw | frame pointer |
| ra[13] | 32 | 0 | rw | |
| zero[14] | 32 | 0 | r- | constant zero |
| at[14] | 32 | 0 | rw | |
| v0[14] | 32 | 0 | rw | |
| v1[14] | 32 | 0 | rw | |
| a0[14] | 32 | 0 | rw | |
| a1[14] | 32 | 0 | rw | |
| a2[14] | 32 | 0 | rw | |
| a3[14] | 32 | 0 | rw | |
| t0[14] | 32 | 0 | rw | |
| t1[14] | 32 | 0 | rw | |
| t2[14] | 32 | 0 | rw | |
| t3[14] | 32 | 0 | rw | |
| t4[14] | 32 | 0 | rw | |

| | | | | |
|----------|----|---|----|---------------|
| t5[14] | 32 | 0 | rw | |
| t6[14] | 32 | 0 | rw | |
| t7[14] | 32 | 0 | rw | |
| s0[14] | 32 | 0 | rw | |
| s1[14] | 32 | 0 | rw | |
| s2[14] | 32 | 0 | rw | |
| s3[14] | 32 | 0 | rw | |
| s4[14] | 32 | 0 | rw | |
| s5[14] | 32 | 0 | rw | |
| s6[14] | 32 | 0 | rw | |
| s7[14] | 32 | 0 | rw | |
| t8[14] | 32 | 0 | rw | |
| t9[14] | 32 | 0 | rw | |
| k0[14] | 32 | 0 | rw | |
| k1[14] | 32 | 0 | rw | |
| gp[14] | 32 | 0 | rw | |
| sp[14] | 32 | 0 | rw | stack pointer |
| s8[14] | 32 | 0 | rw | frame pointer |
| ra[14] | 32 | 0 | rw | |
| zero[15] | 32 | 0 | r- | constant zero |
| at[15] | 32 | 0 | rw | |
| v0[15] | 32 | 0 | rw | |
| v1[15] | 32 | 0 | rw | |
| a0[15] | 32 | 0 | rw | |
| a1[15] | 32 | 0 | rw | |
| a2[15] | 32 | 0 | rw | |
| a3[15] | 32 | 0 | rw | |
| t0[15] | 32 | 0 | rw | |
| t1[15] | 32 | 0 | rw | |
| t2[15] | 32 | 0 | rw | |
| t3[15] | 32 | 0 | rw | |
| t4[15] | 32 | 0 | rw | |
| t5[15] | 32 | 0 | rw | |
| t6[15] | 32 | 0 | rw | |
| t7[15] | 32 | 0 | rw | |
| s0[15] | 32 | 0 | rw | |
| s1[15] | 32 | 0 | rw | |
| s2[15] | 32 | 0 | rw | |
| s3[15] | 32 | 0 | rw | |
| s4[15] | 32 | 0 | rw | |
| s5[15] | 32 | 0 | rw | |
| s6[15] | 32 | 0 | rw | |
| s7[15] | 32 | 0 | rw | |
| t8[15] | 32 | 0 | rw | |
| t9[15] | 32 | 0 | rw | |
| k0[15] | 32 | 0 | rw | |
| k1[15] | 32 | 0 | rw | |
| gp[15] | 32 | 0 | rw | |
| sp[15] | 32 | 0 | rw | stack pointer |
| s8[15] | 32 | 0 | rw | frame pointer |
| ra[15] | 32 | 0 | rw | |
| r0[0] | 32 | 0 | r- | constant zero |
| r1[0] | 32 | 0 | rw | |
| r2[0] | 32 | 0 | rw | |
| r3[0] | 32 | 0 | rw | |
| r4[0] | 32 | 0 | rw | |

| | | | | |
|--------|----|---|----|---------------|
| r5[0] | 32 | 0 | rw | |
| r6[0] | 32 | 0 | rw | |
| r7[0] | 32 | 0 | rw | |
| r8[0] | 32 | 0 | rw | |
| r9[0] | 32 | 0 | rw | |
| r10[0] | 32 | 0 | rw | |
| r11[0] | 32 | 0 | rw | |
| r12[0] | 32 | 0 | rw | |
| r13[0] | 32 | 0 | rw | |
| r14[0] | 32 | 0 | rw | |
| r15[0] | 32 | 0 | rw | |
| r16[0] | 32 | 0 | rw | |
| r17[0] | 32 | 0 | rw | |
| r18[0] | 32 | 0 | rw | |
| r19[0] | 32 | 0 | rw | |
| r20[0] | 32 | 0 | rw | |
| r21[0] | 32 | 0 | rw | |
| r22[0] | 32 | 0 | rw | |
| r23[0] | 32 | 0 | rw | |
| r24[0] | 32 | 0 | rw | |
| r25[0] | 32 | 0 | rw | |
| r26[0] | 32 | 0 | rw | |
| r27[0] | 32 | 0 | rw | |
| r28[0] | 32 | 0 | rw | |
| r29[0] | 32 | 0 | rw | stack pointer |
| r30[0] | 32 | 0 | rw | frame pointer |
| r31[0] | 32 | 0 | rw | |
| r0[1] | 32 | 0 | r- | constant zero |
| r1[1] | 32 | 0 | rw | |
| r2[1] | 32 | 0 | rw | |
| r3[1] | 32 | 0 | rw | |
| r4[1] | 32 | 0 | rw | |
| r5[1] | 32 | 0 | rw | |
| r6[1] | 32 | 0 | rw | |
| r7[1] | 32 | 0 | rw | |
| r8[1] | 32 | 0 | rw | |
| r9[1] | 32 | 0 | rw | |
| r10[1] | 32 | 0 | rw | |
| r11[1] | 32 | 0 | rw | |
| r12[1] | 32 | 0 | rw | |
| r13[1] | 32 | 0 | rw | |
| r14[1] | 32 | 0 | rw | |
| r15[1] | 32 | 0 | rw | |
| r16[1] | 32 | 0 | rw | |
| r17[1] | 32 | 0 | rw | |
| r18[1] | 32 | 0 | rw | |
| r19[1] | 32 | 0 | rw | |
| r20[1] | 32 | 0 | rw | |
| r21[1] | 32 | 0 | rw | |
| r22[1] | 32 | 0 | rw | |
| r23[1] | 32 | 0 | rw | |
| r24[1] | 32 | 0 | rw | |
| r25[1] | 32 | 0 | rw | |
| r26[1] | 32 | 0 | rw | |
| r27[1] | 32 | 0 | rw | |
| r28[1] | 32 | 0 | rw | |

| | | | | |
|--------|----|---|----|---------------|
| r29[1] | 32 | 0 | rw | stack pointer |
| r30[1] | 32 | 0 | rw | frame pointer |
| r31[1] | 32 | 0 | rw | |
| r0[2] | 32 | 0 | r- | constant zero |
| r1[2] | 32 | 0 | rw | |
| r2[2] | 32 | 0 | rw | |
| r3[2] | 32 | 0 | rw | |
| r4[2] | 32 | 0 | rw | |
| r5[2] | 32 | 0 | rw | |
| r6[2] | 32 | 0 | rw | |
| r7[2] | 32 | 0 | rw | |
| r8[2] | 32 | 0 | rw | |
| r9[2] | 32 | 0 | rw | |
| r10[2] | 32 | 0 | rw | |
| r11[2] | 32 | 0 | rw | |
| r12[2] | 32 | 0 | rw | |
| r13[2] | 32 | 0 | rw | |
| r14[2] | 32 | 0 | rw | |
| r15[2] | 32 | 0 | rw | |
| r16[2] | 32 | 0 | rw | |
| r17[2] | 32 | 0 | rw | |
| r18[2] | 32 | 0 | rw | |
| r19[2] | 32 | 0 | rw | |
| r20[2] | 32 | 0 | rw | |
| r21[2] | 32 | 0 | rw | |
| r22[2] | 32 | 0 | rw | |
| r23[2] | 32 | 0 | rw | |
| r24[2] | 32 | 0 | rw | |
| r25[2] | 32 | 0 | rw | |
| r26[2] | 32 | 0 | rw | |
| r27[2] | 32 | 0 | rw | |
| r28[2] | 32 | 0 | rw | |
| r29[2] | 32 | 0 | rw | stack pointer |
| r30[2] | 32 | 0 | rw | frame pointer |
| r31[2] | 32 | 0 | rw | |
| r0[3] | 32 | 0 | r- | constant zero |
| r1[3] | 32 | 0 | rw | |
| r2[3] | 32 | 0 | rw | |
| r3[3] | 32 | 0 | rw | |
| r4[3] | 32 | 0 | rw | |
| r5[3] | 32 | 0 | rw | |
| r6[3] | 32 | 0 | rw | |
| r7[3] | 32 | 0 | rw | |
| r8[3] | 32 | 0 | rw | |
| r9[3] | 32 | 0 | rw | |
| r10[3] | 32 | 0 | rw | |
| r11[3] | 32 | 0 | rw | |
| r12[3] | 32 | 0 | rw | |
| r13[3] | 32 | 0 | rw | |
| r14[3] | 32 | 0 | rw | |
| r15[3] | 32 | 0 | rw | |
| r16[3] | 32 | 0 | rw | |
| r17[3] | 32 | 0 | rw | |
| r18[3] | 32 | 0 | rw | |
| r19[3] | 32 | 0 | rw | |
| r20[3] | 32 | 0 | rw | |

| | | | | |
|--------|----|---|----|---------------|
| r21[3] | 32 | 0 | rw | |
| r22[3] | 32 | 0 | rw | |
| r23[3] | 32 | 0 | rw | |
| r24[3] | 32 | 0 | rw | |
| r25[3] | 32 | 0 | rw | |
| r26[3] | 32 | 0 | rw | |
| r27[3] | 32 | 0 | rw | |
| r28[3] | 32 | 0 | rw | |
| r29[3] | 32 | 0 | rw | stack pointer |
| r30[3] | 32 | 0 | rw | frame pointer |
| r31[3] | 32 | 0 | rw | |
| r0[4] | 32 | 0 | r- | constant zero |
| r1[4] | 32 | 0 | rw | |
| r2[4] | 32 | 0 | rw | |
| r3[4] | 32 | 0 | rw | |
| r4[4] | 32 | 0 | rw | |
| r5[4] | 32 | 0 | rw | |
| r6[4] | 32 | 0 | rw | |
| r7[4] | 32 | 0 | rw | |
| r8[4] | 32 | 0 | rw | |
| r9[4] | 32 | 0 | rw | |
| r10[4] | 32 | 0 | rw | |
| r11[4] | 32 | 0 | rw | |
| r12[4] | 32 | 0 | rw | |
| r13[4] | 32 | 0 | rw | |
| r14[4] | 32 | 0 | rw | |
| r15[4] | 32 | 0 | rw | |
| r16[4] | 32 | 0 | rw | |
| r17[4] | 32 | 0 | rw | |
| r18[4] | 32 | 0 | rw | |
| r19[4] | 32 | 0 | rw | |
| r20[4] | 32 | 0 | rw | |
| r21[4] | 32 | 0 | rw | |
| r22[4] | 32 | 0 | rw | |
| r23[4] | 32 | 0 | rw | |
| r24[4] | 32 | 0 | rw | |
| r25[4] | 32 | 0 | rw | |
| r26[4] | 32 | 0 | rw | |
| r27[4] | 32 | 0 | rw | |
| r28[4] | 32 | 0 | rw | |
| r29[4] | 32 | 0 | rw | stack pointer |
| r30[4] | 32 | 0 | rw | frame pointer |
| r31[4] | 32 | 0 | rw | |
| r0[5] | 32 | 0 | r- | constant zero |
| r1[5] | 32 | 0 | rw | |
| r2[5] | 32 | 0 | rw | |
| r3[5] | 32 | 0 | rw | |
| r4[5] | 32 | 0 | rw | |
| r5[5] | 32 | 0 | rw | |
| r6[5] | 32 | 0 | rw | |
| r7[5] | 32 | 0 | rw | |
| r8[5] | 32 | 0 | rw | |
| r9[5] | 32 | 0 | rw | |
| r10[5] | 32 | 0 | rw | |
| r11[5] | 32 | 0 | rw | |
| r12[5] | 32 | 0 | rw | |

| | | | | |
|--------|----|---|----|---------------|
| r13[5] | 32 | 0 | rw | |
| r14[5] | 32 | 0 | rw | |
| r15[5] | 32 | 0 | rw | |
| r16[5] | 32 | 0 | rw | |
| r17[5] | 32 | 0 | rw | |
| r18[5] | 32 | 0 | rw | |
| r19[5] | 32 | 0 | rw | |
| r20[5] | 32 | 0 | rw | |
| r21[5] | 32 | 0 | rw | |
| r22[5] | 32 | 0 | rw | |
| r23[5] | 32 | 0 | rw | |
| r24[5] | 32 | 0 | rw | |
| r25[5] | 32 | 0 | rw | |
| r26[5] | 32 | 0 | rw | |
| r27[5] | 32 | 0 | rw | |
| r28[5] | 32 | 0 | rw | |
| r29[5] | 32 | 0 | rw | stack pointer |
| r30[5] | 32 | 0 | rw | frame pointer |
| r31[5] | 32 | 0 | rw | |
| r0[6] | 32 | 0 | r- | constant zero |
| r1[6] | 32 | 0 | rw | |
| r2[6] | 32 | 0 | rw | |
| r3[6] | 32 | 0 | rw | |
| r4[6] | 32 | 0 | rw | |
| r5[6] | 32 | 0 | rw | |
| r6[6] | 32 | 0 | rw | |
| r7[6] | 32 | 0 | rw | |
| r8[6] | 32 | 0 | rw | |
| r9[6] | 32 | 0 | rw | |
| r10[6] | 32 | 0 | rw | |
| r11[6] | 32 | 0 | rw | |
| r12[6] | 32 | 0 | rw | |
| r13[6] | 32 | 0 | rw | |
| r14[6] | 32 | 0 | rw | |
| r15[6] | 32 | 0 | rw | |
| r16[6] | 32 | 0 | rw | |
| r17[6] | 32 | 0 | rw | |
| r18[6] | 32 | 0 | rw | |
| r19[6] | 32 | 0 | rw | |
| r20[6] | 32 | 0 | rw | |
| r21[6] | 32 | 0 | rw | |
| r22[6] | 32 | 0 | rw | |
| r23[6] | 32 | 0 | rw | |
| r24[6] | 32 | 0 | rw | |
| r25[6] | 32 | 0 | rw | |
| r26[6] | 32 | 0 | rw | |
| r27[6] | 32 | 0 | rw | |
| r28[6] | 32 | 0 | rw | |
| r29[6] | 32 | 0 | rw | stack pointer |
| r30[6] | 32 | 0 | rw | frame pointer |
| r31[6] | 32 | 0 | rw | |
| r0[7] | 32 | 0 | r- | constant zero |
| r1[7] | 32 | 0 | rw | |
| r2[7] | 32 | 0 | rw | |
| r3[7] | 32 | 0 | rw | |
| r4[7] | 32 | 0 | rw | |

| | | | | |
|--------|----|---|----|---------------|
| r5[7] | 32 | 0 | rw | |
| r6[7] | 32 | 0 | rw | |
| r7[7] | 32 | 0 | rw | |
| r8[7] | 32 | 0 | rw | |
| r9[7] | 32 | 0 | rw | |
| r10[7] | 32 | 0 | rw | |
| r11[7] | 32 | 0 | rw | |
| r12[7] | 32 | 0 | rw | |
| r13[7] | 32 | 0 | rw | |
| r14[7] | 32 | 0 | rw | |
| r15[7] | 32 | 0 | rw | |
| r16[7] | 32 | 0 | rw | |
| r17[7] | 32 | 0 | rw | |
| r18[7] | 32 | 0 | rw | |
| r19[7] | 32 | 0 | rw | |
| r20[7] | 32 | 0 | rw | |
| r21[7] | 32 | 0 | rw | |
| r22[7] | 32 | 0 | rw | |
| r23[7] | 32 | 0 | rw | |
| r24[7] | 32 | 0 | rw | |
| r25[7] | 32 | 0 | rw | |
| r26[7] | 32 | 0 | rw | |
| r27[7] | 32 | 0 | rw | |
| r28[7] | 32 | 0 | rw | |
| r29[7] | 32 | 0 | rw | stack pointer |
| r30[7] | 32 | 0 | rw | frame pointer |
| r31[7] | 32 | 0 | rw | |
| r0[8] | 32 | 0 | r- | constant zero |
| r1[8] | 32 | 0 | rw | |
| r2[8] | 32 | 0 | rw | |
| r3[8] | 32 | 0 | rw | |
| r4[8] | 32 | 0 | rw | |
| r5[8] | 32 | 0 | rw | |
| r6[8] | 32 | 0 | rw | |
| r7[8] | 32 | 0 | rw | |
| r8[8] | 32 | 0 | rw | |
| r9[8] | 32 | 0 | rw | |
| r10[8] | 32 | 0 | rw | |
| r11[8] | 32 | 0 | rw | |
| r12[8] | 32 | 0 | rw | |
| r13[8] | 32 | 0 | rw | |
| r14[8] | 32 | 0 | rw | |
| r15[8] | 32 | 0 | rw | |
| r16[8] | 32 | 0 | rw | |
| r17[8] | 32 | 0 | rw | |
| r18[8] | 32 | 0 | rw | |
| r19[8] | 32 | 0 | rw | |
| r20[8] | 32 | 0 | rw | |
| r21[8] | 32 | 0 | rw | |
| r22[8] | 32 | 0 | rw | |
| r23[8] | 32 | 0 | rw | |
| r24[8] | 32 | 0 | rw | |
| r25[8] | 32 | 0 | rw | |
| r26[8] | 32 | 0 | rw | |
| r27[8] | 32 | 0 | rw | |
| r28[8] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| r29[8] | 32 | 0 | rw | stack pointer |
| r30[8] | 32 | 0 | rw | frame pointer |
| r31[8] | 32 | 0 | rw | |
| r0[9] | 32 | 0 | r- | constant zero |
| r1[9] | 32 | 0 | rw | |
| r2[9] | 32 | 0 | rw | |
| r3[9] | 32 | 0 | rw | |
| r4[9] | 32 | 0 | rw | |
| r5[9] | 32 | 0 | rw | |
| r6[9] | 32 | 0 | rw | |
| r7[9] | 32 | 0 | rw | |
| r8[9] | 32 | 0 | rw | |
| r9[9] | 32 | 0 | rw | |
| r10[9] | 32 | 0 | rw | |
| r11[9] | 32 | 0 | rw | |
| r12[9] | 32 | 0 | rw | |
| r13[9] | 32 | 0 | rw | |
| r14[9] | 32 | 0 | rw | |
| r15[9] | 32 | 0 | rw | |
| r16[9] | 32 | 0 | rw | |
| r17[9] | 32 | 0 | rw | |
| r18[9] | 32 | 0 | rw | |
| r19[9] | 32 | 0 | rw | |
| r20[9] | 32 | 0 | rw | |
| r21[9] | 32 | 0 | rw | |
| r22[9] | 32 | 0 | rw | |
| r23[9] | 32 | 0 | rw | |
| r24[9] | 32 | 0 | rw | |
| r25[9] | 32 | 0 | rw | |
| r26[9] | 32 | 0 | rw | |
| r27[9] | 32 | 0 | rw | |
| r28[9] | 32 | 0 | rw | |
| r29[9] | 32 | 0 | rw | stack pointer |
| r30[9] | 32 | 0 | rw | frame pointer |
| r31[9] | 32 | 0 | rw | |
| r0[10] | 32 | 0 | r- | constant zero |
| r1[10] | 32 | 0 | rw | |
| r2[10] | 32 | 0 | rw | |
| r3[10] | 32 | 0 | rw | |
| r4[10] | 32 | 0 | rw | |
| r5[10] | 32 | 0 | rw | |
| r6[10] | 32 | 0 | rw | |
| r7[10] | 32 | 0 | rw | |
| r8[10] | 32 | 0 | rw | |
| r9[10] | 32 | 0 | rw | |
| r10[10] | 32 | 0 | rw | |
| r11[10] | 32 | 0 | rw | |
| r12[10] | 32 | 0 | rw | |
| r13[10] | 32 | 0 | rw | |
| r14[10] | 32 | 0 | rw | |
| r15[10] | 32 | 0 | rw | |
| r16[10] | 32 | 0 | rw | |
| r17[10] | 32 | 0 | rw | |
| r18[10] | 32 | 0 | rw | |
| r19[10] | 32 | 0 | rw | |
| r20[10] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| r21[10] | 32 | 0 | rw | |
| r22[10] | 32 | 0 | rw | |
| r23[10] | 32 | 0 | rw | |
| r24[10] | 32 | 0 | rw | |
| r25[10] | 32 | 0 | rw | |
| r26[10] | 32 | 0 | rw | |
| r27[10] | 32 | 0 | rw | |
| r28[10] | 32 | 0 | rw | |
| r29[10] | 32 | 0 | rw | stack pointer |
| r30[10] | 32 | 0 | rw | frame pointer |
| r31[10] | 32 | 0 | rw | |
| r0[11] | 32 | 0 | r- | constant zero |
| r1[11] | 32 | 0 | rw | |
| r2[11] | 32 | 0 | rw | |
| r3[11] | 32 | 0 | rw | |
| r4[11] | 32 | 0 | rw | |
| r5[11] | 32 | 0 | rw | |
| r6[11] | 32 | 0 | rw | |
| r7[11] | 32 | 0 | rw | |
| r8[11] | 32 | 0 | rw | |
| r9[11] | 32 | 0 | rw | |
| r10[11] | 32 | 0 | rw | |
| r11[11] | 32 | 0 | rw | |
| r12[11] | 32 | 0 | rw | |
| r13[11] | 32 | 0 | rw | |
| r14[11] | 32 | 0 | rw | |
| r15[11] | 32 | 0 | rw | |
| r16[11] | 32 | 0 | rw | |
| r17[11] | 32 | 0 | rw | |
| r18[11] | 32 | 0 | rw | |
| r19[11] | 32 | 0 | rw | |
| r20[11] | 32 | 0 | rw | |
| r21[11] | 32 | 0 | rw | |
| r22[11] | 32 | 0 | rw | |
| r23[11] | 32 | 0 | rw | |
| r24[11] | 32 | 0 | rw | |
| r25[11] | 32 | 0 | rw | |
| r26[11] | 32 | 0 | rw | |
| r27[11] | 32 | 0 | rw | |
| r28[11] | 32 | 0 | rw | |
| r29[11] | 32 | 0 | rw | stack pointer |
| r30[11] | 32 | 0 | rw | frame pointer |
| r31[11] | 32 | 0 | rw | |
| r0[12] | 32 | 0 | r- | constant zero |
| r1[12] | 32 | 0 | rw | |
| r2[12] | 32 | 0 | rw | |
| r3[12] | 32 | 0 | rw | |
| r4[12] | 32 | 0 | rw | |
| r5[12] | 32 | 0 | rw | |
| r6[12] | 32 | 0 | rw | |
| r7[12] | 32 | 0 | rw | |
| r8[12] | 32 | 0 | rw | |
| r9[12] | 32 | 0 | rw | |
| r10[12] | 32 | 0 | rw | |
| r11[12] | 32 | 0 | rw | |
| r12[12] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| r13[12] | 32 | 0 | rw | |
| r14[12] | 32 | 0 | rw | |
| r15[12] | 32 | 0 | rw | |
| r16[12] | 32 | 0 | rw | |
| r17[12] | 32 | 0 | rw | |
| r18[12] | 32 | 0 | rw | |
| r19[12] | 32 | 0 | rw | |
| r20[12] | 32 | 0 | rw | |
| r21[12] | 32 | 0 | rw | |
| r22[12] | 32 | 0 | rw | |
| r23[12] | 32 | 0 | rw | |
| r24[12] | 32 | 0 | rw | |
| r25[12] | 32 | 0 | rw | |
| r26[12] | 32 | 0 | rw | |
| r27[12] | 32 | 0 | rw | |
| r28[12] | 32 | 0 | rw | |
| r29[12] | 32 | 0 | rw | stack pointer |
| r30[12] | 32 | 0 | rw | frame pointer |
| r31[12] | 32 | 0 | rw | |
| r0[13] | 32 | 0 | r- | constant zero |
| r1[13] | 32 | 0 | rw | |
| r2[13] | 32 | 0 | rw | |
| r3[13] | 32 | 0 | rw | |
| r4[13] | 32 | 0 | rw | |
| r5[13] | 32 | 0 | rw | |
| r6[13] | 32 | 0 | rw | |
| r7[13] | 32 | 0 | rw | |
| r8[13] | 32 | 0 | rw | |
| r9[13] | 32 | 0 | rw | |
| r10[13] | 32 | 0 | rw | |
| r11[13] | 32 | 0 | rw | |
| r12[13] | 32 | 0 | rw | |
| r13[13] | 32 | 0 | rw | |
| r14[13] | 32 | 0 | rw | |
| r15[13] | 32 | 0 | rw | |
| r16[13] | 32 | 0 | rw | |
| r17[13] | 32 | 0 | rw | |
| r18[13] | 32 | 0 | rw | |
| r19[13] | 32 | 0 | rw | |
| r20[13] | 32 | 0 | rw | |
| r21[13] | 32 | 0 | rw | |
| r22[13] | 32 | 0 | rw | |
| r23[13] | 32 | 0 | rw | |
| r24[13] | 32 | 0 | rw | |
| r25[13] | 32 | 0 | rw | |
| r26[13] | 32 | 0 | rw | |
| r27[13] | 32 | 0 | rw | |
| r28[13] | 32 | 0 | rw | |
| r29[13] | 32 | 0 | rw | stack pointer |
| r30[13] | 32 | 0 | rw | frame pointer |
| r31[13] | 32 | 0 | rw | |
| r0[14] | 32 | 0 | r- | constant zero |
| r1[14] | 32 | 0 | rw | |
| r2[14] | 32 | 0 | rw | |
| r3[14] | 32 | 0 | rw | |
| r4[14] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| r5[14] | 32 | 0 | rw | |
| r6[14] | 32 | 0 | rw | |
| r7[14] | 32 | 0 | rw | |
| r8[14] | 32 | 0 | rw | |
| r9[14] | 32 | 0 | rw | |
| r10[14] | 32 | 0 | rw | |
| r11[14] | 32 | 0 | rw | |
| r12[14] | 32 | 0 | rw | |
| r13[14] | 32 | 0 | rw | |
| r14[14] | 32 | 0 | rw | |
| r15[14] | 32 | 0 | rw | |
| r16[14] | 32 | 0 | rw | |
| r17[14] | 32 | 0 | rw | |
| r18[14] | 32 | 0 | rw | |
| r19[14] | 32 | 0 | rw | |
| r20[14] | 32 | 0 | rw | |
| r21[14] | 32 | 0 | rw | |
| r22[14] | 32 | 0 | rw | |
| r23[14] | 32 | 0 | rw | |
| r24[14] | 32 | 0 | rw | |
| r25[14] | 32 | 0 | rw | |
| r26[14] | 32 | 0 | rw | |
| r27[14] | 32 | 0 | rw | |
| r28[14] | 32 | 0 | rw | |
| r29[14] | 32 | 0 | rw | stack pointer |
| r30[14] | 32 | 0 | rw | frame pointer |
| r31[14] | 32 | 0 | rw | |
| r0[15] | 32 | 0 | r- | constant zero |
| r1[15] | 32 | 0 | rw | |
| r2[15] | 32 | 0 | rw | |
| r3[15] | 32 | 0 | rw | |
| r4[15] | 32 | 0 | rw | |
| r5[15] | 32 | 0 | rw | |
| r6[15] | 32 | 0 | rw | |
| r7[15] | 32 | 0 | rw | |
| r8[15] | 32 | 0 | rw | |
| r9[15] | 32 | 0 | rw | |
| r10[15] | 32 | 0 | rw | |
| r11[15] | 32 | 0 | rw | |
| r12[15] | 32 | 0 | rw | |
| r13[15] | 32 | 0 | rw | |
| r14[15] | 32 | 0 | rw | |
| r15[15] | 32 | 0 | rw | |
| r16[15] | 32 | 0 | rw | |
| r17[15] | 32 | 0 | rw | |
| r18[15] | 32 | 0 | rw | |
| r19[15] | 32 | 0 | rw | |
| r20[15] | 32 | 0 | rw | |
| r21[15] | 32 | 0 | rw | |
| r22[15] | 32 | 0 | rw | |
| r23[15] | 32 | 0 | rw | |
| r24[15] | 32 | 0 | rw | |
| r25[15] | 32 | 0 | rw | |
| r26[15] | 32 | 0 | rw | |
| r27[15] | 32 | 0 | rw | |
| r28[15] | 32 | 0 | rw | |

| | | | | |
|---------|----|---|----|---------------|
| r29[15] | 32 | 0 | rw | stack pointer |
| r30[15] | 32 | 0 | rw | frame pointer |
| r31[15] | 32 | 0 | rw | |

Table 13.4: Registers at level 1, type:CPU group:Shadow

13.1.5 COP0

Registers at level:1, type:CPU group:COP0

| Name | Bits | Initial-Hex | RW | Description |
|--------------|------|-------------|----|-----------------------------|
| sr | 32 | 400004 | rw | CP0 register 12/0 (status) |
| bad | 32 | 0 | rw | CP0 register 8/0 (badvaddr) |
| cause | 32 | 0 | rw | CP0 register 13/0 (cause) |
| index | 32 | 0 | rw | CP0 register 0/0 |
| random | 32 | 0 | rw | CP0 register 1/0 |
| entrylo0 | 32 | 0 | rw | CP0 register 2/0 |
| entrylo1 | 32 | 0 | rw | CP0 register 3/0 |
| context | 32 | 0 | rw | CP0 register 4/0 |
| userlocal | 32 | 0 | rw | CP0 register 4/2 |
| pagemask | 32 | 0 | rw | CP0 register 5/0 |
| pagegrain | 32 | 0 | rw | CP0 register 5/1 |
| wired | 32 | 0 | rw | CP0 register 6/0 |
| hwrena | 32 | 0 | rw | CP0 register 7/0 |
| badvaddr | 32 | 0 | rw | CP0 register 8/0 |
| badinstr | 32 | 0 | rw | CP0 register 8/1 |
| badinstrp | 32 | 0 | rw | CP0 register 8/2 |
| count | 32 | 0 | rw | CP0 register 9/0 |
| entryhi | 32 | 0 | rw | CP0 register 10/0 |
| guestctl1 | 32 | 0 | rw | CP0 register 10/4 |
| guestctl2 | 32 | 0 | rw | CP0 register 10/5 |
| guestctl3 | 32 | 0 | rw | CP0 register 10/6 |
| compare | 32 | 0 | rw | CP0 register 11/0 |
| guestctl0ext | 32 | 40 | rw | CP0 register 11/4 |
| status | 32 | 400004 | rw | CP0 register 12/0 |
| intctl | 32 | e3830000 | rw | CP0 register 12/1 |
| srstctl | 32 | 3c000000 | rw | CP0 register 12/2 |
| srsmap | 32 | 0 | rw | CP0 register 12/3 |
| viewipl | 32 | 0 | rw | CP0 register 12/4 |
| srsmap2 | 32 | 0 | rw | CP0 register 12/5 |
| guestctl0 | 32 | c4c00fc | rw | CP0 register 12/6 |
| gtoffset | 32 | 0 | rw | CP0 register 12/7 |
| viewripl | 32 | 0 | rw | CP0 register 13/4 |
| nestedexc | 32 | 0 | rw | CP0 register 13/5 |
| epc | 32 | 0 | rw | CP0 register 14/0 |
| nestedepc | 32 | 0 | rw | CP0 register 14/2 |
| prid | 32 | 1a720 | rw | CP0 register 15/0 |
| ebase | 32 | 80000000 | rw | CP0 register 15/1 |
| cdmmbase | 32 | 0 | rw | CP0 register 15/2 |
| config | 32 | 81a08482 | rw | CP0 register 16/0 |
| config1 | 32 | bf1a4d03 | rw | CP0 register 16/1 |
| config2 | 32 | 80000000 | rw | CP0 register 16/2 |
| config3 | 32 | 8ca2bc28 | rw | CP0 register 16/3 |
| config4 | 32 | a00c0000 | rw | CP0 register 16/4 |
| config5 | 32 | 1 | rw | CP0 register 16/5 |
| config6 | 32 | 0 | rw | CP0 register 16/6 |

| | | | | |
|-------------------|----|----------|----|-------------------------|
| config7 | 32 | 80040000 | rw | CP0 register 16/7 |
| lladdr | 32 | 0 | rw | CP0 register 17/0 |
| debug | 32 | 2028000 | rw | CP0 register 23/0 |
| depc | 32 | 0 | rw | CP0 register 24/0 |
| errctl | 32 | 0 | rw | CP0 register 26/0 |
| itaglo | 32 | 0 | rw | CP0 register 28/0 |
| idatalo | 32 | 0 | rw | CP0 register 28/1 |
| dtaglo | 32 | 0 | rw | CP0 register 28/2 |
| ddatalo | 32 | 0 | rw | CP0 register 28/3 |
| l23taglo | 32 | 0 | rw | CP0 register 28/4 |
| l23datalo | 32 | 0 | rw | CP0 register 28/5 |
| itaghi | 32 | 0 | rw | CP0 register 29/0 |
| idatahi | 32 | 0 | rw | CP0 register 29/1 |
| dtaghi | 32 | 0 | rw | CP0 register 29/2 |
| l23datahi | 32 | 0 | rw | CP0 register 29/5 |
| errorepc | 32 | 0 | rw | CP0 register 30/0 |
| desave | 32 | 0 | rw | CP0 register 31/0 |
| kscratch1 | 32 | 0 | rw | CP0 register 31/2 |
| kscratch2 | 32 | 0 | rw | CP0 register 31/3 |
| guestindex | 32 | 0 | rw | CP0 guest register 0/0 |
| guestrandom | 32 | 0 | rw | CP0 guest register 1/0 |
| guestentrylo0 | 32 | 0 | rw | CP0 guest register 2/0 |
| guestentrylo1 | 32 | 0 | rw | CP0 guest register 3/0 |
| guestcontext | 32 | 0 | rw | CP0 guest register 4/0 |
| guestuserlocal | 32 | 0 | rw | CP0 guest register 4/2 |
| guestpagemask | 32 | 0 | rw | CP0 guest register 5/0 |
| guestpagegrain | 32 | 0 | rw | CP0 guest register 5/1 |
| guestwired | 32 | 0 | rw | CP0 guest register 6/0 |
| guesthwrena | 32 | 0 | rw | CP0 guest register 7/0 |
| guestbadvaddr | 32 | 0 | rw | CP0 guest register 8/0 |
| guestbadinstr | 32 | 0 | rw | CP0 guest register 8/1 |
| guestbadinstrp | 32 | 0 | rw | CP0 guest register 8/2 |
| guestcount | 32 | 0 | rw | CP0 guest register 9/0 |
| guestentryhi | 32 | 0 | rw | CP0 guest register 10/0 |
| guestguestctl1 | 32 | 0 | rw | CP0 guest register 10/4 |
| guestguestctl2 | 32 | 0 | rw | CP0 guest register 10/5 |
| guestguestctl3 | 32 | 0 | rw | CP0 guest register 10/6 |
| guestcompare | 32 | 0 | rw | CP0 guest register 11/0 |
| guestguestctl0ext | 32 | 0 | rw | CP0 guest register 11/4 |
| gueststatus | 32 | 400004 | rw | CP0 guest register 12/0 |
| guestintctl | 32 | e3830000 | rw | CP0 guest register 12/1 |
| guestsrctl | 32 | 3c000000 | rw | CP0 guest register 12/2 |
| guestsrsmmap | 32 | 0 | rw | CP0 guest register 12/3 |
| guestviewipl | 32 | 0 | rw | CP0 guest register 12/4 |
| guestsrsmmap2 | 32 | 0 | rw | CP0 guest register 12/5 |
| guestguestctl0 | 32 | 0 | rw | CP0 guest register 12/6 |
| guestgtoffset | 32 | 0 | rw | CP0 guest register 12/7 |
| guestcause | 32 | 0 | rw | CP0 guest register 13/0 |
| guestviewripl | 32 | 0 | rw | CP0 guest register 13/4 |
| guestnestedexc | 32 | 0 | rw | CP0 guest register 13/5 |
| guestepc | 32 | 0 | rw | CP0 guest register 14/0 |
| guestnestedepc | 32 | 0 | rw | CP0 guest register 14/2 |
| guestprid | 32 | 0 | rw | CP0 guest register 15/0 |
| guestbase | 32 | 80000000 | rw | CP0 guest register 15/1 |
| guestcdmmbase | 32 | 0 | rw | CP0 guest register 15/2 |
| guestconfig | 32 | 81a08482 | rw | CP0 guest register 16/0 |

| | | | | |
|----------------|----|----------|----|-------------------------|
| guestconfig1 | 32 | bf1a4d01 | rw | CP0 guest register 16/1 |
| guestconfig2 | 32 | 80000000 | rw | CP0 guest register 16/2 |
| guestconfig3 | 32 | 8c22bc20 | rw | CP0 guest register 16/3 |
| guestconfig4 | 32 | a00c0000 | rw | CP0 guest register 16/4 |
| guestconfig5 | 32 | 1 | rw | CP0 guest register 16/5 |
| guestconfig6 | 32 | 0 | rw | CP0 guest register 16/6 |
| guestconfig7 | 32 | 0 | rw | CP0 guest register 16/7 |
| guestlladdr | 32 | 0 | rw | CP0 guest register 17/0 |
| guestdebug | 32 | 0 | rw | CP0 guest register 23/0 |
| guestdepc | 32 | 0 | rw | CP0 guest register 24/0 |
| guesterrctl | 32 | 0 | rw | CP0 guest register 26/0 |
| guestitaglo | 32 | 0 | rw | CP0 guest register 28/0 |
| guestidatalo | 32 | 0 | rw | CP0 guest register 28/1 |
| guestdtaglo | 32 | 0 | rw | CP0 guest register 28/2 |
| guestddatalo | 32 | 0 | rw | CP0 guest register 28/3 |
| guestl23taglo | 32 | 0 | rw | CP0 guest register 28/4 |
| guestl23datalo | 32 | 0 | rw | CP0 guest register 28/5 |
| guestitaghi | 32 | 0 | rw | CP0 guest register 29/0 |
| guestidatahi | 32 | 0 | rw | CP0 guest register 29/1 |
| guestdtaghi | 32 | 0 | rw | CP0 guest register 29/2 |
| guestl23datahi | 32 | 0 | rw | CP0 guest register 29/5 |
| guesterrorepc | 32 | 0 | rw | CP0 guest register 30/0 |
| guestdesave | 32 | 0 | rw | CP0 guest register 31/0 |
| guestkscratch1 | 32 | 0 | rw | CP0 guest register 31/2 |
| guestkscratch2 | 32 | 0 | rw | CP0 guest register 31/3 |

Table 13.5: Registers at level 1, type:CPU group:COP0

13.1.6 SPRAM

Registers at level:1, type:CPU group:SPRAM

| Name | Bits | Initial-Hex | RW | Description |
|---------------|------|-------------|----|-------------|
| ISPRAM_INDEX | 8 | 0 | rw | |
| ISPRAM_ENABLE | 8 | 0 | rw | |
| ISPRAM_SIZE | 8 | 0 | rw | |
| ISPRAM_BASE | 64 | 0 | rw | |
| ISPRAM_OFFSET | 32 | 0 | rw | |
| ISPRAM_FILE | 64 | - | -w | |
| ISPRAM_READ | 32 | - | -w | |
| ISPRAM_WRITE | 32 | - | -w | |
| DSPRAM_INDEX | 8 | 0 | rw | |
| DSPRAM_ENABLE | 8 | 0 | rw | |
| DSPRAM_SIZE | 8 | 0 | rw | |
| DSPRAM_BASE | 64 | 0 | rw | |
| DSPRAM_OFFSET | 32 | 0 | rw | |
| DSPRAM_READ | 32 | - | -w | |
| DSPRAM_WRITE | 32 | - | -w | |

Table 13.6: Registers at level 1, type:CPU group:SPRAM

13.1.7 Integration support

Registers at level:1, type:CPU group:Integration_support

| Name | Bits | Initial-Hex | RW | Description |
|------|------|-------------|----|---------------------------------------|
| stop | 32 | 0 | rw | write with non-zero to stop processor |

Table 13.7: Registers at level 1, type:CPU group:Integration.support