



## OVP Guide to Using Processor Models

### Model specific information for MIPS\_24KEf

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## Model Release Status

This model is released as part of OVP releases and is included in OVPworld packages. Please visit [OVPworld.org](http://OVPworld.org).

# Contents

|           |                                   |           |
|-----------|-----------------------------------|-----------|
| <b>1</b>  | <b>Overview</b>                   | <b>1</b>  |
| 1.1       | Description . . . . .             | 1         |
| 1.2       | Licensing . . . . .               | 1         |
| 1.3       | Limitations . . . . .             | 1         |
| 1.4       | Verification . . . . .            | 2         |
| 1.5       | Features . . . . .                | 2         |
| <b>2</b>  | <b>Configuration</b>              | <b>3</b>  |
| 2.1       | Location . . . . .                | 3         |
| 2.2       | GDB Path . . . . .                | 3         |
| 2.3       | Semi-Host Library . . . . .       | 3         |
| 2.4       | Processor Endian-ness . . . . .   | 3         |
| 2.5       | QuantumLeap Support . . . . .     | 3         |
| 2.6       | Processor ELF code . . . . .      | 3         |
| <b>3</b>  | <b>All Variants in this model</b> | <b>4</b>  |
| <b>4</b>  | <b>Bus Master Ports</b>           | <b>6</b>  |
| <b>5</b>  | <b>Bus Slave Ports</b>            | <b>7</b>  |
| <b>6</b>  | <b>Net Ports</b>                  | <b>8</b>  |
| <b>7</b>  | <b>FIFO Ports</b>                 | <b>9</b>  |
| <b>8</b>  | <b>Formal Parameters</b>          | <b>10</b> |
| <b>9</b>  | <b>Execution Modes</b>            | <b>14</b> |
| <b>10</b> | <b>Exceptions</b>                 | <b>15</b> |
| <b>11</b> | <b>Hierarchy of the model</b>     | <b>16</b> |
| 11.1      | Level 1: CPU . . . . .            | 16        |
| <b>12</b> | <b>Model Commands</b>             | <b>17</b> |
| 12.1      | Level 1: CPU . . . . .            | 17        |
| 12.1.1    | isync . . . . .                   | 17        |
| 12.1.2    | itrace . . . . .                  | 17        |
| 12.1.3    | mipsCOP0 . . . . .                | 17        |

|           |                      |           |
|-----------|----------------------|-----------|
| 12.1.4    | mipsCacheDisable     | 18        |
| 12.1.4.1  | Argument description | 18        |
| 12.1.5    | mipsCacheEnable      | 18        |
| 12.1.6    | mipsCacheRatio       | 18        |
| 12.1.7    | mipsCacheReport      | 18        |
| 12.1.7.1  | Argument description | 18        |
| 12.1.8    | mipsCacheReset       | 18        |
| 12.1.8.1  | Argument description | 18        |
| 12.1.9    | mipsCacheTrace       | 18        |
| 12.1.10   | mipsDebugFlags       | 19        |
| 12.1.11   | mipsReadRegister     | 19        |
| 12.1.12   | mipsReadTLBEntry     | 19        |
| 12.1.13   | mipsTLBDump          | 19        |
| 12.1.13.1 | Argument description | 19        |
| 12.1.14   | mipsTLBGetPhys       | 19        |
| 12.1.15   | mipsWriteRegister    | 20        |
| 12.1.16   | mipsWriteTLBEntry    | 20        |
| <b>13</b> | <b>Registers</b>     | <b>21</b> |
| 13.1      | Level 1: CPU         | 21        |
| 13.1.1    | Core                 | 21        |
| 13.1.2    | FPU                  | 22        |
| 13.1.3    | DSP                  | 22        |
| 13.1.4    | COP0                 | 23        |
| 13.1.5    | Integration_support  | 24        |

# Chapter 1

## Overview

This document provides the details of an OVP Fast Processor Model variant.

OVP Fast Processor Models are written in C and provide a C API for use in C based platforms. The models also provide a native interface for use in SystemC TLM2 platforms.

The models are written using the OVP VMI API that provides a Virtual Machine Interface that defines the behavior of the processor. The VMI API makes a clear line between model and simulator allowing very good optimization and world class high speed performance. Most models are provided as a binary shared object and also as source. This allows the download and use of the model binary or the use of the source to explore and modify the model.

The models are run through an extensive QA and regression testing process and most model families are validated using technology provided by the processor IP owners. There is a companion document (OVP Guide to Using Processor Models) which explains the general concepts of OVP Fast Processor Models and their use. It is downloadable from the OVPworld website documentation pages.

### 1.1 Description

MIPS32 Configurable Processor Model

### 1.2 Licensing

Usage of binary model under license governing simulator usage. Source of model available under Imperas Software License Agreement.

### 1.3 Limitations

If this model is not part of your installation, then it is available for download from [www.OVPworld.org/MIPUser](http://www.OVPworld.org/MIPUser).

## 1.4 Verification

Models have been validated correct as part of the MIPS Verified program and run through the MIPS AVP test programs

## 1.5 Features

only MIPS32 Instruction set implemented

MMU Type: Standard TLB

FPU implemented

L1 I and D cache model in either full or tag-only mode implemented (disabled by default)

Vectored interrupts implemented

MIPS16e ASE implemented

DSP ASE implemented

# Chapter 2

## Configuration

### 2.1 Location

This model's VLVN is `mips.ovpworld.org/processor/mips32_r1r5/1.0`.

The model source is usually at:

`$IMPERAS_HOME/ImperasLib/source/mips.ovpworld.org/processor/mips32_r1r5/1.0`

The model binary is usually at:

`$IMPERAS_HOME/lib/$IMPERAS_ARCH/ImperasLib/mips.ovpworld.org/processor/mips32_r1r5/1.0`

### 2.2 GDB Path

The default GDB for this model is: `$IMPERAS_HOME/lib/$IMPERAS_ARCH/gdb/mips-sde-elf-gdb`.

### 2.3 Semi-Host Library

The default semi-host library file is `mips.ovpworld.org/semihosting/mips32Newlib/1.0`

### 2.4 Processor Endian-ness

This model can be set to either endian-ness (normally by a pin, or the ELF code).

### 2.5 QuantumLeap Support

This processor is qualified to run in a QuantumLeap enabled simulator.

### 2.6 Processor ELF code

The ELF code supported by this model is: `0x8`.

## Chapter 3

# All Variants in this model

This model has these variants

| <b>Variant</b> | Description                  |
|----------------|------------------------------|
| ISA            |                              |
| M14K           |                              |
| M14KcTLB       |                              |
| M14KcFMM       |                              |
| 4KEc           |                              |
| 4KEm           |                              |
| 4KEp           |                              |
| M4K            |                              |
| 4Kc            |                              |
| 4Km            |                              |
| 4Kp            |                              |
| 24Kc           |                              |
| 24Kf           |                              |
| 24KEc          |                              |
| 24KEf          | (described in this document) |
| 34Kc           |                              |
| 34Kf           |                              |
| 34Kn           |                              |
| 74Kc           |                              |
| 74Kf           |                              |
| 1004Kc         |                              |
| 1004Kf         |                              |
| 1074Kc         |                              |
| 1074Kf         |                              |
| microAptivC    |                              |
| microAptivP    |                              |
| microAptivCF   |                              |
| interAptiv     |                              |
| interAptivUP   |                              |
| proAptiv       |                              |



---

Table 3.1: All Variants in this model

## Chapter 4

# Bus Master Ports

This model has these bus master ports.

| <b>Name</b> | min | max | Connect?  | Description |
|-------------|-----|-----|-----------|-------------|
| INSTRUCTION | 12  | 36  | mandatory |             |
| DATA        | 12  | 36  | optional  |             |

Table 4.1: Bus Master Ports

## Chapter 5

# Bus Slave Ports

This model has no bus slave ports.

## Chapter 6

# Net Ports

This model has these net ports.

| Name                | Type  | Connect? | Description  |
|---------------------|-------|----------|--|
| reset               | input | optional | Core reset   |
| dint                | input | optional | Debug external interrupt   |
| SI_UseExceptionBase | input | optional | SI_UseExceptionBase input<br>(mask=0x00000001)                               |
| SI_ExceptionBase    | input | optional | SI_ExceptionBase input<br>(mask=0xffff000)                                   |
| hwint0              | input | optional | External interrupt   |
| hwint1              | input | optional | External interrupt   |
| hwint2              | input | optional | External interrupt   |
| hwint3              | input | optional | External interrupt   |
| hwint4              | input | optional | External interrupt   |
| hwint5              | input | optional | External interrupt   |
| nmi                 | input | optional | Non-maskable external interrupt  |
| vc_run              | input | optional | Set to force stop of execution on processor<br>VPE (simulation control only) |

Table 6.1: Net Ports

## Chapter 7

# FIFO Ports

This model has no FIFO ports.

## Chapter 8

# Formal Parameters

| Name                     | Type        | Description  |
|--------------------------|-------------|--|
| variant                  | Enumeration | Processor variant  |
| endian                   | Endian      | Model endian   |
| cacheenable              | Enumeration | Select cache model mode (default, tag or full)   |
| cachedebug               | Uns32       | Cache debug flags  |
| cacheextbiuinfo          | Pointer     | Pointer to platform-provided BIU cache info structure  |
| mipsHexFile              | String      | Load a MIPS hex file (test-mode)   |
| IMPERAS_MIPS_AVP_OPCODES | Boolean     | Enable MIPS-specific magic Pass/Fail opcodes (specific for AVP test termination)   |
| cacheIndexBypassTLB      | Boolean     | When set, cache index ops do not generate TLB exceptions   |
| MIPS_TRACE               | Boolean     | Enable MIPS-format trace output  |
| supervisorMode           | Boolean     | Override whether processor implements supervisor mode  |
| busErrors                | Boolean     | Override bus error exception behavior. When true, accesses of memory not defined by platform will cause bus error exceptions |
| fixedMMU                 | Boolean     | Override the MMU type to fixed mapping when true (sets Config.MT=3, Config.KU/K23=2 and Config1.MMUSizeM1=0)                 |
| removeDSP                | Boolean     | Override the DSP-present configuration when true (sets Config3.DSPP/DSP2P=0)   |
| removeCMP                | Boolean     | Override the CMP-Present configuration when true (sets Config3.CMGCR and GCR_BASE to 0)                                      |
| removeFP                 | Boolean     | Override the FP-Present configuration when true (sets Config1.FP to 0)   |
| isISA                    | Boolean     | Enable to specify ISA model (reset address from ELF, all coprocessors enabled)   |
| hiddenTLBentries         | Boolean     | Deprecated - Instead set config1MMUSizeM1 to maximum value to improve performance  |
| ITCNumEntries            | Uns32       | Specify number of ITC cells present (MT cores only)  |
| ITCNumFIFO               | Uns32       | Specify number of ITC FIFO cells in reference ITC implementation (MT cores only)   |
| MTFPU                    | Uns32       | Enable multi-threaded FPU (1:old mttc1 behavior, 2:new mttc1 behavior)   |
| supportDenormals         | Boolean     | Enable to specify that the FPU supports denormal operands and results  |
| VPE0MaxTC                | Uns32       | Specifies the maximum TCs initially on VPE0  |
| mpuRegions               | Uns32       | Number of regions for memory protection unit   |
| mpuType                  | Uns32       | Type of MPU implementation   |
| mpuEnable                | Boolean     | Enable MPU2 segment control at reset   |
| mpuSegment0              | Uns32       | Attributes for segment 0 in MPU2 SegmentControl.0 register   |

|              |         |   |
|--------------|---------|---|
| mpuSegment1  | Uns32   | Attributes for segment 1 in MPU2 SegmentControl_0 register          |
| mpuSegment2  | Uns32   | Attributes for segment 2 in MPU2 SegmentControl_0 register          |
| mpuSegment3  | Uns32   | Attributes for segment 3 in MPU2 SegmentControl_0 register          |
| mpuSegment4  | Uns32   | Attributes for segment 4 in MPU2 SegmentControl_1 register          |
| mpuSegment5  | Uns32   | Attributes for segment 5 in MPU2 SegmentControl_1 register          |
| mpuSegment6  | Uns32   | Attributes for segment 6 in MPU2 SegmentControl_1 register          |
| mpuSegment7  | Uns32   | Attributes for segment 7 in MPU2 SegmentControl_1 register          |
| mpuSegment8  | Uns32   | Attributes for segment 8 in MPU2 SegmentControl_2 register          |
| mpuSegment9  | Uns32   | Attributes for segment 9 in MPU2 SegmentControl_2 register          |
| mpuSegment10 | Uns32   | Attributes for segment 10 in MPU2 SegmentControl_2 register         |
| mpuSegment11 | Uns32   | Attributes for segment 11 in MPU2 SegmentControl_2 register         |
| mpuSegment12 | Uns32   | Attributes for segment 12 in MPU2 SegmentControl_3 register         |
| mpuSegment13 | Uns32   | Attributes for segment 13 in MPU2 SegmentControl_3 register         |
| mpuSegment14 | Uns32   | Attributes for segment 14 in MPU2 SegmentControl_3 register         |
| mpuSegment15 | Uns32   | Attributes for segment 15 in MPU2 SegmentControl_3 register         |
| mvpconf0vpe  | Uns32   | Override MVPConf0.PVPE  |
| mvpconf0tc   | Uns32   | Override MVPConf0.PTC   |
| mvpconf0pcp  | Boolean | Override MVPConf0.PCP   |
| mvpconf0tcp  | Boolean | Override MVPConf0.TCP   |
| hasFDC       | Uns32   | Specify the size of Fast Debug Channel register block               |
| statusFR     | Boolean | Override power on value in Status.FR (Floating point register mode) |
| configDSP    | Boolean | Override Config.DSP (data scratchpad RAM present)                   |
| configISP    | Boolean | Override Config.ISP (instruction scratchpad RAM present)            |
| configK0     | Uns32   | Override power on value of Config.K0 (set Kseg0 cacheability)       |
| configKU     | Uns32   | Override power on value of Config.KU (set Useg cacheability)        |
| configK23    | Uns32   | Override power on value of Config.K23 (set Kseg23 cacheability)     |
| configMDU    | Boolean | Override Config.MDU (iterative multiply/divide unit)                |
| configMM     | Boolean | Override Config.MM (merging mode for write)                         |
| configMT     | Uns32   | Override Config.MT  |
| configSB     | Boolean | Override Config.SB (simple bus transfers only)                      |
| MIPS16eASE   | Boolean | Override Config1.CA (enables the MIPS16e ASE)                       |
| config1DA    | Uns32   | Override Config1.DA (Dcache associativity)                          |
| config1DL    | Uns32   | Override Config1.DL (Dcache line size)                              |
| config1DS    | Uns32   | Override Config1.DS (Dcache sets per way)                           |
| config1EP    | Boolean | Override Config1.EP (EJTag present)                                 |
| config1IA    | Uns32   | Override Config1.IA (Icache associativity)                          |

|                    |         |   |
|--------------------|---------|---|
| config1IL          | Uns32   | Override Config1.IL (Icache line size)  |
| config1IS          | Uns32   | Override Config1.IS (Icache sets per way)   |
| config1MMUSizeM1   | Uns32   | Override Config1.MMUSizeM1 (number of MMU entries-1)                              |
| config1WR          | Boolean | Override Config1.WR (watchpoint registers present)                                |
| config1FP          | Boolean | Override Config1.FP (FPU present)   |
| config3BI          | Boolean | Override Config3.BI   |
| config3BP          | Boolean | Override Config3.BP   |
| config3CDMM        | Boolean | Override Config3.CDMM   |
| config3CTXTC       | Boolean | Override Config3.CTXTC  |
| config3DSPP        | Boolean | Override Config3.DSPP   |
| config3DSP2P       | Boolean | Override Config3.DSP2P  |
| config3IPLW        | Uns32   | Override Config3.IPLW   |
| config3ISA         | Uns32   | Override Config3.ISA  |
| config3ISAOnExc    | Boolean | Override Config3.ISAOnExc   |
| config3ITL         | Boolean | Override Config3.ITL  |
| config3MCU         | Boolean | Override Config3.MCU  |
| config3MMAR        | Uns32   | Override Config3.MMAR   |
| config3RXI         | Boolean | Override Config3.RXI  |
| config3SC          | Boolean | Override Config3.SC   |
| config3ULRI        | Boolean | Override Config3.ULRI   |
| externalinterrupt  | Boolean | Override Config3.VEIC (enables the use of an external interrupt controller)       |
| vectoredinterrupt  | Boolean | Override Config3.VInt (enables vectored interrupts)                               |
| config3VZ          | Boolean | Override Config3.VZ   |
| config4AE          | Boolean | Override Config4.AE   |
| config4IE          | Uns32   | Override Config4.IE   |
| config4MMUConfig   | Uns32   | Override Config4.MMUConfig field (interpretation depends on MMUExtDef value)      |
| config4MMUExtDef   | Uns32   | Override Config4.MMUExtDef  |
| config4VTLBSizeExt | Uns32   | Override Config4.VTLBSizeExt  |
| config5EVA         | Boolean | Override Config5.EVA  |
| config5NFExists    | Boolean | Override Config5.NFExists   |
| config5MSAEn       | Boolean | Override Config5.MSAEn  |
| config6FTLBEEn     | Boolean | Override power on value of Config6.FTLBEEn  |
| config7AR          | Boolean | Override Config7.AR (Alias removed Data cache)                                    |
| config7DCIDX_MODE  | Uns32   | Override Config7.DCIDX_MODE   |
| config7HCI         | Boolean | Override Config7.HCI (Hardware Cache Initialization)                              |
| config7IAR         | Boolean | Override Config7.IAR (Alias removed Instruction cache)                            |
| config7WII         | Boolean | Override Config7.WII (wait IE/IXMT ignore)  |
| fcsrABS2008        | Boolean | Override FCSR.ABS2008 (ABS/NEG compliant with IEEE 754-2008)                      |
| fcsrNaN2008        | Boolean | Override FCSR.NaN2008 (QNaN/SNaN encodings match IEEE 754-2008 recommendation)    |
| firPS              | Boolean | Override FIR.PS (PS floating point type implemented)                              |
| firHas2008         | Boolean | Override FIR.Has2008 (one or more IEEE 754-2008 features present)                 |
| intctlIPFDC        | Uns32   | Override IntCtl.IPFDC   |
| intctlIPTI         | Uns32   | Override IntCtl.IPTI  |
| pridRevision       | Uns32   | Override PRId.Revision  |
| srsctlHSS          | Uns32   | Override SRSCtl.HSS (number of shadow register sets)                              |
| ExceptionBase      | Uns32   | Specify the BEV Exception Base address. (use GCR_Cx_RESET_BASE on CMP processors) |
| UseExceptionBase   | Boolean | Set to one to use ExceptionBase[29:12] as the corresponding BEV address bits      |



|                              |         |  |
|------------------------------|---------|--|
| firstBEVExceptionBaseMaskBit | Uns32   | Specify LSB position of GCR_Cx_RESET_EXT_BASE. BEVExceptionBaseMask field. Only used when SegCtl present                       |
| EVAReset                     | Boolean | Set to one to reset into non-legacy address map and BEV location. Only used when non-CMP and SegCtl present                    |
| ExceptionBaseMask            | Uns32   | Specify the ExceptionBaseMask value used for bits [27:firstBEVExceptionBaseMaskBit]. Only used when non-CMP and SegCtl present |
| ExceptionBasePA              | Uns32   | Bits [35:29] of the physical address for the BEV overlays. Only used when non-CMP and SegCtl present                           |
| EIC_OPTION                   | Uns32   | Override the external interrupt controller EIC_OPTION  |
| ISPRAM_SIZE                  | Uns32   | Encoded size of the ISPRAM region ( $\log_2(\text{ISPRAM size in bytes}) - 11$ )   |
| ISPRAM_BASE                  | Uns64   | Starting physical address of the ISPRAM region   |
| ISPRAM_ENABLE                | Boolean | Set the enable bit of the ISPRAM region's tag (used to enable the ISPRAM region prior to reset)                                |
| ISPRAM_FILE                  | String  | Load a MIPS hex file into the ISPRAM region prior to reset   |
| DSPRAM_SIZE                  | Uns32   | Encoded size of the DSPRAM region ( $\log_2(\text{DSPRAM size in bytes}) - 11$ )   |
| DSPRAM_BASE                  | Uns64   | Starting physical address of the DSPRAM region   |
| DSPRAM_ENABLE                | Boolean | Set the enable bit of the DSPRAM region's tag (used to enable the DSPRAM region prior to reset)                                |

Table 8.1: Parameters that can be set in: CPU

## Chapter 9

# Execution Modes

| Mode       | Code |
|------------|------|
| KERNEL     | 0    |
| DEBUG      | 1    |
| SUPERVISOR | 2    |
| USER       | 3    |

Table 9.1: Modes implemented in: CPU

# Chapter 10

## Exceptions

| Exception | Code |
|-----------|------|
| Int       | 0    |
| Mod       | 1    |
| TLBL      | 2    |
| TLBS      | 3    |
| AdEL      | 4    |
| AdES      | 5    |
| IBE       | 6    |
| DBE       | 7    |
| Sys       | 8    |
| Bp        | 9    |
| RI        | 10   |
| CpU       | 11   |
| Ov        | 12   |
| Tr        | 13   |
| FPE       | 15   |
| Impl1     | 16   |
| Impl2     | 17   |
| C2E       | 18   |
| TLBRI     | 19   |
| TLBXI     | 20   |
| MDMX      | 22   |
| WATCH     | 23   |
| MCheck    | 24   |
| Thread    | 25   |
| DSPDis    | 26   |
| Prot      | 29   |
| CacheErr  | 30   |

Table 10.1: Exceptions implemented in: CPU

# Chapter 11

## Hierarchy of the model

A CPU core may be configured to instance many processors of a Symmetrical Multi Processor (SMP). A CPU core may also have sub elements within a processor, for example hardware threading blocks.

OVP processor models can be written to include SMP blocks and to have many levels of hierarchy. Some OVP CPU models may have a fixed hierarchy, and some may be configured by settings in a configuration register. Please see the register definitions of this model.

This model documentation shows the settings and hierarchy of the default settings for this model variant.

### 11.1 Level 1: CPU

This level in the model hierarchy has 16 commands.

This level in the model hierarchy has 5 register groups:

| Group name          | Registers |
|---------------------|-----------|
| Core                | 33        |
| FPU                 | 34        |
| DSP                 | 9         |
| COP0                | 43        |
| Integration_support | 1         |

Table 11.1: Register groups

This level in the model hierarchy has no children.

# Chapter 12

## Model Commands

A Processor model can implement one or more **Model Commands** available to be invoked from the simulator command line, from the OP API or from the Imperas Multiprocessor Debugger.

### 12.1 Level 1: CPU

#### 12.1.1 isync

specify instruction address range for synchronous execution

| Argument   | Type  | Description                                  |
|------------|-------|--|
| -addresshi | Uns64 | end address of synchronous execution range   |
| -addresslo | Uns64 | start address of synchronous execution range |

Table 12.1: isync command arguments

#### 12.1.2 itrace

enable or disable instruction tracing

| Argument          | Type    | Description                                  |
|-------------------|---------|--|
| -after            | Uns64   | apply after this many instructions           |
| -enable           | Boolean | enable instruction tracing                   |
| -instructioncount | Boolean | include the instruction number in each trace |
| -off              | Boolean | disable instruction tracing                  |
| -on               | Boolean | enable instruction tracing                   |
| -registerchange   | Boolean | show registers changed by this instruction   |
| -registers        | Boolean | show registers after each trace              |

Table 12.2: itrace command arguments

#### 12.1.3 mipsCOP0

query a COP0 register value using <register><select>

| Argument  | Type  | Description                      |
|-----------|-------|----------------------------------|
| -register | Uns32 | specify the COP0 register number |

|         |       |                                  |
|---------|-------|----------------------------------|
| -select | Uns32 | specify the COP0 register select |
|---------|-------|----------------------------------|

Table 12.3: mipsCOP0 command arguments

## 12.1.4 mipsCacheDisable

### 12.1.4.1 Argument description

Disables tag or full cache model

## 12.1.5 mipsCacheEnable

enable tag or full cache model

| Argument | Type    | Description                      |
|----------|---------|----------------------------------|
| -debug   | Uns32   | set cache model debug flags      |
| -full    | Boolean | enable full cache model          |
| -tag     | Boolean | enable cache tag line only model |

Table 12.4: mipsCacheEnable command arguments

## 12.1.6 mipsCacheRatio

Report current hit ratio for selected cache

| Argument | Type    | Description                 |
|----------|---------|-----------------------------|
| -dcache  | Boolean | report hit ratio for dcache |
| -icache  | Boolean | report hit ratio for icache |

Table 12.5: mipsCacheRatio command arguments

## 12.1.7 mipsCacheReport

### 12.1.7.1 Argument description

Report current cache statistics

## 12.1.8 mipsCacheReset

### 12.1.8.1 Argument description

reset the cache model

## 12.1.9 mipsCacheTrace

Control the tracing of cache accesses

| Argument    | Type    | Description              |
|-------------|---------|--------------------------|
| -noartifact | Boolean | filter artifact accesses |
| -nocached   | Boolean | filter cached accesses   |
| -nodcache   | Boolean | filter dcache accesses   |

|             |         |                            |
|-------------|---------|----------------------------|
| -noicache   | Boolean | filter icache accesses     |
| -notrue     | Boolean | filter true accesses       |
| -nouncached | Boolean | filter uncached accesses   |
| -off        | Boolean | turn off the cache tracing |
| -on         | Boolean | turn on the cache tracing  |

Table 12.6: mipsCacheTrace command arguments

### 12.1.10 mipsDebugFlags

Set the processor model debug flags to <value>

| Argument | Type  | Description               |
|----------|-------|---------------------------|
| -value   | Uns32 | specify model debug flags |

Table 12.7: mipsDebugFlags command arguments

### 12.1.11 mipsReadRegister

Read a processor register using <resource><offset>

| Argument  | Type  | Description                            |
|-----------|-------|--|
| -offset   | Uns32 | the processor register offset          |
| -resource | Uns32 | the processor register resource number |

Table 12.8: mipsReadRegister command arguments

### 12.1.12 mipsReadTLBEntry

read a TLB entry specified by the index

| Argument | Type  | Description          |
|----------|-------|----------------------|
| -index   | Uns64 | select the TLB entry |

Table 12.9: mipsReadTLBEntry command arguments

### 12.1.13 mipsTLBDump

#### 12.1.13.1 Argument description

Dumps the current contents of the TLB

### 12.1.14 mipsTLBGetPhys

Reports the entry(s) in the TLB that match the given virtual address and ASID

| Argument | Type  | Description     |
|----------|-------|-----------------|
| -asid    | Uns64 | ASID            |
| -va      | Uns64 | virtual address |

Table 12.10: mipsTLBGetPhys command arguments

### 12.1.15 mipsWriteRegister

Write to a processor register using <resource><offset><value>

| Argument  | Type  | Description                      |
|-----------|-------|----------------------------------|
| -offset   | Uns32 | the register offset number       |
| -resource | Uns32 | the register resource number     |
| -value    | Uns64 | the register value to be written |

Table 12.11: mipsWriteRegister command arguments

### 12.1.16 mipsWriteTLBEntry

Writes values to a TLB entry using the index, lo0, lo1, hi0 and mask fields

| Argument | Type  | Description                 |
|----------|-------|-----------------------------|
| -hi0     | Uns64 | the TLB entry high address  |
| -index   | Uns64 | the TLB entry index         |
| -lo0     | Uns64 | the TLB entry low address 0 |
| -lo1     | Uns64 | the TLB entry low address 1 |
| -mask    | Uns64 | the TLB entry mask          |

Table 12.12: mipsWriteTLBEntry command arguments



# Chapter 13

## Registers

### 13.1 Level 1: CPU

#### 13.1.1 Core

Registers at level:1, type:CPU group:Core

| Name | Bits | Initial-Hex | RW | Description     |
|------|------|-------------|----|-----------------|
| zero | 32   | 0           | r- | constant zero   |
| at   | 32   | 0           | rw |                 |
| v0   | 32   | 0           | rw |                 |
| v1   | 32   | 0           | rw |                 |
| a0   | 32   | 0           | rw |                 |
| a1   | 32   | 0           | rw |                 |
| a2   | 32   | 0           | rw |                 |
| a3   | 32   | 0           | rw |                 |
| t0   | 32   | 0           | rw |                 |
| t1   | 32   | 0           | rw |                 |
| t2   | 32   | 0           | rw |                 |
| t3   | 32   | 0           | rw |                 |
| t4   | 32   | 0           | rw |                 |
| t5   | 32   | 0           | rw |                 |
| t6   | 32   | 0           | rw |                 |
| t7   | 32   | 0           | rw |                 |
| s0   | 32   | 0           | rw |                 |
| s1   | 32   | 0           | rw |                 |
| s2   | 32   | 0           | rw |                 |
| s3   | 32   | 0           | rw |                 |
| s4   | 32   | 0           | rw |                 |
| s5   | 32   | 0           | rw |                 |
| s6   | 32   | 0           | rw |                 |
| s7   | 32   | 0           | rw |                 |
| t8   | 32   | 0           | rw |                 |
| t9   | 32   | 0           | rw |                 |
| k0   | 32   | 0           | rw |                 |
| k1   | 32   | 0           | rw |                 |
| gp   | 32   | 0           | rw |                 |
| sp   | 32   | 0           | rw | stack pointer   |
| s8   | 32   | 0           | rw | frame pointer   |
| ra   | 32   | 0           | rw |                 |
| pc   | 32   | bfc00000    | rw | program counter |

Table 13.1: Registers at level 1, type:CPU group:Core

### 13.1.2 FPU

Registers at level:1, type:CPU group:FPU

| Name | Bits | Initial-Hex | RW | Description                |
|------|------|-------------|----|----------------------------|
| f0   | 32   | 0           | rw |                            |
| f1   | 32   | 0           | rw |                            |
| f2   | 32   | 0           | rw |                            |
| f3   | 32   | 0           | rw |                            |
| f4   | 32   | 0           | rw |                            |
| f5   | 32   | 0           | rw |                            |
| f6   | 32   | 0           | rw |                            |
| f7   | 32   | 0           | rw |                            |
| f8   | 32   | 0           | rw |                            |
| f9   | 32   | 0           | rw |                            |
| f10  | 32   | 0           | rw |                            |
| f11  | 32   | 0           | rw |                            |
| f12  | 32   | 0           | rw |                            |
| f13  | 32   | 0           | rw |                            |
| f14  | 32   | 0           | rw |                            |
| f15  | 32   | 0           | rw |                            |
| f16  | 32   | 0           | rw |                            |
| f17  | 32   | 0           | rw |                            |
| f18  | 32   | 0           | rw |                            |
| f19  | 32   | 0           | rw |                            |
| f20  | 32   | 0           | rw |                            |
| f21  | 32   | 0           | rw |                            |
| f22  | 32   | 0           | rw |                            |
| f23  | 32   | 0           | rw |                            |
| f24  | 32   | 0           | rw |                            |
| f25  | 32   | 0           | rw |                            |
| f26  | 32   | 0           | rw |                            |
| f27  | 32   | 0           | rw |                            |
| f28  | 32   | 0           | rw |                            |
| f29  | 32   | 0           | rw |                            |
| f30  | 32   | 0           | rw |                            |
| f31  | 32   | 0           | rw |                            |
| fsr  | 32   | 0           | rw | floating point status      |
| fir  | 32   | 739600      | r- | floating point information |

Table 13.2: Registers at level 1, type:CPU group:FPU

### 13.1.3 DSP

Registers at level:1, type:CPU group:DSP

| Name | Bits | Initial-Hex | RW | Description |
|------|------|-------------|----|-------------|
| lo   | 32   | 0           | rw |             |
| hi   | 32   | 0           | rw |             |
| lo1  | 32   | 0           | rw |             |
| hi1  | 32   | 0           | rw |             |
| lo2  | 32   | 0           | rw |             |

|        |    |   |    |             |
|--------|----|---|----|-------------|
| hi2    | 32 | 0 | rw |             |
| lo3    | 32 | 0 | rw |             |
| hi3    | 32 | 0 | rw |             |
| dspctl | 32 | 0 | rw | DSP control |

Table 13.3: Registers at level 1, type:CPU group:DSP

### 13.1.4 COP0

Registers at level:1, type:CPU group:COP0

| Name      | Bits | Initial-Hex | RW | Description                  |
|-----------|------|-------------|----|------------------------------|
| sr        | 32   | 400004      | rw | CP0 register 12/0 (status)   |
| bad       | 32   | 0           | rw | CP0 register 8/0 (badvaaddr) |
| cause     | 32   | 0           | rw | CP0 register 13/0 (cause)    |
| index     | 32   | 0           | rw | CP0 register 0/0             |
| random    | 32   | 0           | rw | CP0 register 1/0             |
| entrylo0  | 32   | 0           | rw | CP0 register 2/0             |
| entrylo1  | 32   | 0           | rw | CP0 register 3/0             |
| context   | 32   | 0           | rw | CP0 register 4/0             |
| userlocal | 32   | 0           | rw | CP0 register 4/2             |
| pagemask  | 32   | 0           | rw | CP0 register 5/0             |
| wired     | 32   | 0           | rw | CP0 register 6/0             |
| hwrena    | 32   | 0           | rw | CP0 register 7/0             |
| badvaddr  | 32   | 0           | rw | CP0 register 8/0             |
| count     | 32   | 0           | rw | CP0 register 9/0             |
| entryhi   | 32   | 0           | rw | CP0 register 10/0            |
| compare   | 32   | 0           | rw | CP0 register 11/0            |
| status    | 32   | 400004      | rw | CP0 register 12/0            |
| intctl    | 32   | e0000000    | rw | CP0 register 12/1            |
| srctl     | 32   | 0           | rw | CP0 register 12/2            |
| srsmap    | 32   | 0           | rw | CP0 register 12/3            |
| epc       | 32   | 0           | rw | CP0 register 14/0            |
| prid      | 32   | 19600       | rw | CP0 register 15/0            |
| ebase     | 32   | 80000000    | rw | CP0 register 15/1            |
| config    | 32   | 80048482    | rw | CP0 register 16/0            |
| config1   | 32   | 9e231187    | rw | CP0 register 16/1            |
| config2   | 32   | 80000000    | rw | CP0 register 16/2            |
| config3   | 32   | 2420        | rw | CP0 register 16/3            |
| config7   | 32   | 80000000    | rw | CP0 register 16/7            |
| debug     | 32   | 2018000     | rw | CP0 register 23/0            |
| depc      | 32   | 0           | rw | CP0 register 24/0            |
| errctl    | 32   | 0           | rw | CP0 register 26/0            |
| itaglo    | 32   | 0           | rw | CP0 register 28/0            |
| idatalo   | 32   | 0           | rw | CP0 register 28/1            |
| dtaglo    | 32   | 0           | rw | CP0 register 28/2            |
| ddatalo   | 32   | 0           | rw | CP0 register 28/3            |
| l23taglo  | 32   | 0           | rw | CP0 register 28/4            |
| l23datalo | 32   | 0           | rw | CP0 register 28/5            |
| itaghi    | 32   | 0           | rw | CP0 register 29/0            |
| idatahi   | 32   | 0           | rw | CP0 register 29/1            |
| dtaghi    | 32   | 0           | rw | CP0 register 29/2            |
| l23datahi | 32   | 0           | rw | CP0 register 29/5            |
| errorepc  | 32   | 0           | rw | CP0 register 30/0            |
| desave    | 32   | 0           | rw | CP0 register 31/0            |

Table 13.4: Registers at level 1, type:CPU group:COP0

### 13.1.5 Integration\_support

Registers at level:1, type:CPU group:Integration\_support

| Name | Bits | Initial-Hex | RW | Description                           |
|------|------|-------------|----|---------------------------------------|
| stop | 32   | 0           | rw | write with non-zero to stop processor |

Table 13.5: Registers at level 1, type:CPU group:Integration\_support